

# Erik S. Chen

Mobile Phone: (650) 704-9284

E-mail: [shuluc@stanford.edu](mailto:shuluc@stanford.edu)

Address: 334 Olmsted Road, Apt. #147, Stanford  
CA-94305, U.S.A.

## EDUCATION

---

- Jun.07 ~ Present **Ph.D. Candidate, Stanford University, EE dept.** **Palo Alto, CA, U.S.A**  
*Advisor: Prof. James D. Plummer*  
• Process technology engineering and device physics
- Sep.05 ~ Jun.07 **Master, Stanford University, EE dept.** **Palo Alto, CA, U.S.A.**  
*Major: Device physics, Process engineering and Circuit design. GPA 4.0/4.0*
- Sep.99 ~ Jun.03 **Bachelor in Science and Engineering, National Taiwan University, EE dept.** **Taipei, Taiwan**  
*Major: Digital/RF Circuit design, Signal Processing and Process Technology. GPA 3.98/4.0*

## HONORS

---

- Sep.03 **Research Creativity Award, National Science Council, R.O.C.**  
*Topic: Integrated Circuit implementation of Voice Synthesizer based on Physical Modeling Structure*
- Sep.02 ~ Jun.03 **Student Research Fellowship, National Science Council, R.O.C.**  
*Topic: Theory, Modeling and Simulation of Acoustic Signal Processing*
- Feb.02 **First Prize, Engineering Student Paper Contest, National Chinese Institute of Engineers**  
*Topic: Dynamic Acoustic Signal Processing –Virtual Symphonic Orchestra*

## WORK EXPERIENCES

---

- Sep.06 ~ Present **Research Assistant, Stanford University, EE dept.** **Palo Alto, CA, U.S.A**  
*Research Group Supervisor: Prof. James D. Plummer*  
• 3D-IC process engineering, recrystallization method of different materials on amorphous substrate  
• Mobility enhancement based on crystal orientation and strain engineering  
• Novel 3D device structure simulation  
• Negative Differential Resistance device (NDR) modeling –RTD simulation
- Jul.06 ~ Sep.06 **Engineer, Taiwan Semiconductor Manufacturing Company (TSMC), limited.** **Hsinchu, Taiwan**  
*Advanced Module Engineering Program, Module Technology Center (MTC)*  
• Strained silicon process engineering and modification  
• Decoupled plasma nitridation (DPN) gate oxide characterization and implementation  
• Flash anneal source/drain process incorporation and dopants diffusion control
- Mar.05 ~ Sep.05 **Engineer, Unitech Corporation, limited** **Taipei, Taiwan**  
*Research and Development Center, Auto Data Collection group*  
• RFID reader implementation  
• RF front end circuit - directional coupler design

## RESEARCH PROJECTS

---

- Apr.07 25nm technology node NMOS design and simulation, course project
- Apr.06 Capacitor-less DRAM analysis and modeling, course project
- Dec.05 Operational Transconductance Amplifier circuit design, course project
- Dec.02 Digital phase lock loop design and layout
- May.02 Radiation of photonic crystals for use in visible light range
- Dec.01 Speech recognition and related data base construction

## PROFESSIONAL SKILLS

---

### Process Technology

- General process flow, E-beam lithography, Plasma Etch, PECVD

### Characterization tool

- Focused Ion Beam, Scanning Electron Microscope

### Simulation software

- Sentaurus, TSUPREM, ADS, HSPICE, MATLAB

### Layout tool

- Cadence

### High level languages

- C, Visual C++, Verilog