

Richard M. Yoo

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353 Serra Mall, Gates 316, Stanford, CA 94305
U.S. Citizen

OBJECTIVE

To seek an internship position.

Broad knowledge in both computer engineering and computer science. Two and a half year work experience as a skilled IT specialist with proven success in system programming and natural language processing. Excellent programming skills. Cooperative, leading, and prudential character as a coworker and a leader. Energetic. Good physical condition: 2nd poom in taekwondo.

EDUCATION

Stanford University, Stanford, CA

Ph.D. Student (September 2008 ~)

GPA 4.0 / 4.3

Research Advisor: Prof. Christos Kozyrakis

Research Focus: Parallel Runtime Designs and Architecture Interactions

Georgia Institute of Technology, Atlanta, GA

Master of Science (2008)

GPA 4.0 / 4.0

Research Advisor: Prof. Hsien-Hsin S. Lee

Research Focus: Transactional Memory, Multi-Core Performance

Thesis Title: Adaptive Transaction Scheduling for Transactional Memory Systems

Relevant Courses

- Advanced Computer Architecture
- Advanced Issues in Computer Architecture
- Computer Aided VLSI System Design
- Compilers and Interpreters

Seoul National University, Seoul, Korea

Bachelor of Science in Electrical Engineering (2003)

GPA 3.79 / 4.3

Accomplishments

- Graduated with honors.
- Also holds a minor degree in mechanical engineering.

HONORS AND AWARDS

- Honorable Mention, National Science Foundation Graduate Research Fellowship Program (2006)
- Recipient, Georgia Institute of Technology Graduate Tuition Waiver (Fall 2005, Spring 2006)
- Recipient, Seoul National University Academic Scholarship (Spring 1999, Fall 2002)

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PROFESSIONAL EXPERIENCES

Samsung Advanced Institute of Technology (SAIT), Yongin, Korea

Intern, Reconfigurable Processor Core Group / System Architecture Lab (June 2008 ~ August 2008)

Mentor: Soojung Ryu, Manager: Jeongwook Kim

Accomplishments

- Defined SIMD ISA extension for SAIT Reconfigurable Processor.
- Implemented and validated SIMD datapath in RTL.

Intel Corporation, Santa Clara, CA

Graduate Intern Technical, Programming Systems Lab / Corporate Technology Group (August 2007 ~ December 2007)

Mentor: Bratin Saha, Manager: Ali-Reza Adl-Tabatabai

Accomplishments

- Optimized McRT software transactional memory performance. (In Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures.)
- 1 patent pending.

Intel Corporation, Hillsboro, OR

Graduate Intern Technical, Middleware Products Division / Software and Solutions Group (May 2006 ~ August 2006)

Mentor: Kingsum Chow and Han Lee, Manager: Anthony Baker

Accomplishments

- Devised an artificial neural network based non-linear modeling methodology to aid SPECjAppServer2004 performance tuning. (In Proceedings of the 2006 IEEE International Symposium on Workload Characterization.)
- Applied principal components analysis and clustering analysis to SPECjvm2007 to devise an improved scoring metric. (In Proceedings of the 2007 IEEE International Symposium on Workload Characterization.)
- Proposed an automated experiment validation / performance anomaly detection system based on data mining.
- Filed 3 invention disclosures.

NHN Corporation, Seoul, Korea

Leading IT company in Korea which serves Korea's most popular web search engine 'Naver'

Specialist, Information Retrieval Laboratory (2003 ~ 2005)

Accomplishments

- Developed an IOCP based NT server system, which showed more than 99% availability for multi-terabytes of data flow.
- Motivated NHN Corp. to establish China and Japan branches by implementing multi-language conversion framework that manages almost all code pages that exist.
- Implemented document replication detection system for over 300 million web pages.
- Significantly reduced operation costs by actively implementing SNMP based monitoring system.
- Implemented automatic text classification system based on Bayesian inference for Naver news service.

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ASSISTANTSHIPS

Stanford University, Stanford, CA

Research Assistantship

- For Prof. Christos Kozyrakis (Fall 2008 ~)
- Studies on parallel runtime designs and architecture interactions.

Georgia Institute of Technology, Atlanta, GA

Research Assistantship

- For Prof. Hsien-Hsin S. Lee (Fall 2006 ~ Spring 2008)
- Studied on the implications of transaction scheduling on transactional memory performance. (In Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures.)
- Studied on the single-thread performance improvement on transactional memory by implementing out-of-order thread-level speculation on top of an underlying transactional memory system. (In the 2008 Workshop on Parallel Execution of Sequential Programs on Multi-Core Architectures.)

Teaching Assistantship

- For Prof. Gabriel H. Loh (Spring 2006, CS 6290 High-Performance Computer Architecture)

NON-REFEREED PUBLICATIONS

Richard M. Yoo.

"Adaptive Transaction Scheduling for Transactional Memory Systems."

Master's Thesis, School of Electrical and Computer Engineering, Georgia Institute of Technology, May 2008.

Richard M. Yoo and Hsien-Hsin S. Lee.

"Adaptive Transaction Scheduling for Transactional Memory Systems."

Technical Report GIT-CERCS-07-04, Georgia Institute of Technology, February 2007.

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REFEREED PUBLICATIONS

Richard M. Yoo, Anthony Romano, and Christos Kozyrakis.

"Phoenix Rebirth: Scalable MapReduce on a Large-Scale Shared-Memory System."

in *Proceedings of the 2009 IEEE International Symposium on Workload Characterization (IISWC)*, pp. 198-207, Austin, TX, October 2009.

Richard M. Yoo and Hsien-Hsin S. Lee.

"Helper Transactions: Enabling Thread-Level Speculation via A Transactional Memory System."

in *the 2008 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA)*, held in conjunction with the *35th ACM/IEEE International Symposium on Computer Architecture (ISCA)*, Beijing, China, June 2008.

Richard M. Yoo and Hsien-Hsin S. Lee.

"Adaptive Transaction Scheduling for Transactional Memory Systems."

in *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines, pp. 169-178, Munich, Germany, June 2008.

Richard M. Yoo, Yang Ni, Adam Welc, Bratin Saha, Ali-Reza Adl-Tabatabai, and Hsien-Hsin S. Lee.

"Kicking the Tires of Software Transactional Memory: Why the Going Gets Tough."

in *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines, pp. 265-274, Munich, Germany, June 2008.

Richard M. Yoo, Hsien-Hsin S. Lee, Han Lee, and Kingsum Chow.

"Hierarchical Means: Single Number Benchmarking with Workload Cluster Analysis."

in *Proceedings of the 2007 IEEE International Symposium on Workload Characterization (IISWC)*, pp. 204-213, Boston, MA, September 2007.

Richard M. Yoo, Han Lee, Kingsum Chow, and Hsien-Hsin S. Lee.

"Constructing a Non-Linear Model with Neural Networks for Workload Characterization."

in *Proceedings of the 2006 IEEE International Symposium on Workload Characterization (IISWC)*, pp. 150-159, San Jose, CA, October 2006.

Weidong Shi, Hsien-Hsin S. Lee, **Richard M. Yoo**, and Alexandra Boldyreva.

"A Digital Rights Enabled Graphics Processing System."

in *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH)*, pp. 17-26, Vienna, Austria, September 2006.

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COMPUTER SKILLS

Processors

Microarchitecture level knowledge of Intel 8051, 80x86, ARM7, MIPS, and SPARC processors.
Actual VHDL implementation of ARM7TDMI core.

Computer Architecture Simulator

Multifacet GEMS, SIMICS, SimpleScalar

Development Environments

Synopsys, Silicon Ensemble, Virtuoso, Altera Max+plus II, Quartus II, Visual Studio 6.0, .Net 2002, 2003, Vi, GDB, Valgrind, CVS, Subversion, Kawa, Rational Purify

Operating Systems

Red Hat Linux 7.3, 9, Solaris 9, 10, Windows Server 2003, Windows 2000 Server, Windows 3.0, 3.1, 95, 98, Windows 2000, Windows XP, MS-DOS, Mac OS 8.7, X, Cygwin

Programming Languages

VHDL, Verilog, C/C++, C#, Java, Visual Basic, PHP, Python, Perl, SML, COM, ActiveX, MFC, ASN.1, HTML, XML, RSS, Atom, NewsML, DocBook, GW-BASIC

Data mining / natural language processing concepts

Decision Tree Classifiers, Artificial Neural Networks, Self-Organizing Feature Maps, Naïve Bayesian Classifier, Bayesian Networks, Weka, GNU S, MSBNx, Web Document Replication, Document Clustering, Index Building, Thesaurus and Ontology Contracture, Automatic Key Phrase Extraction

Networking

TCP/IP, UDP, DNS, HTTP, SNMP, SAMBA, DHCP, DSL, IOCP, Winsock2, AppleTalk, Active Directory, Apache, IIS

Databases

MySQL, Berkeley DB, Minibase, ODBC

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EXTRA CURRICULAR EVENTS / ACTIVITIES

Seoul National University Photo Club

Served as vice president (2001).

Held three photo exhibitions at the center of the Federation of Art & Cultural Organizations of Korea.

Seoul National University Classic Guitar Symphony

Held two concerts.

Samsung Electronics Cooperative Education Program

Participated in Digital ASIC course.

Mastered skills needed to design production level digital hardware using VHDL.

2nd prize award in 8th National Student Piano Concours

Held by Eumag Chunchu Publishing Co., a renowned competition for promising classical artists in Korea.

2nd Poom in Taekwondo

LICENSES

Information Processing Engineer

Qualification by Human Resources Development Service of Korea.

(License Number : 01203070557C)

REFERENCES

Prof. Christos Kozyrakis

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