


Are Analog Designers Hopeless at Scaling?

Will digital designers eat their lunch at 45nm and below?

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"Dead" people
eating my
lunch?

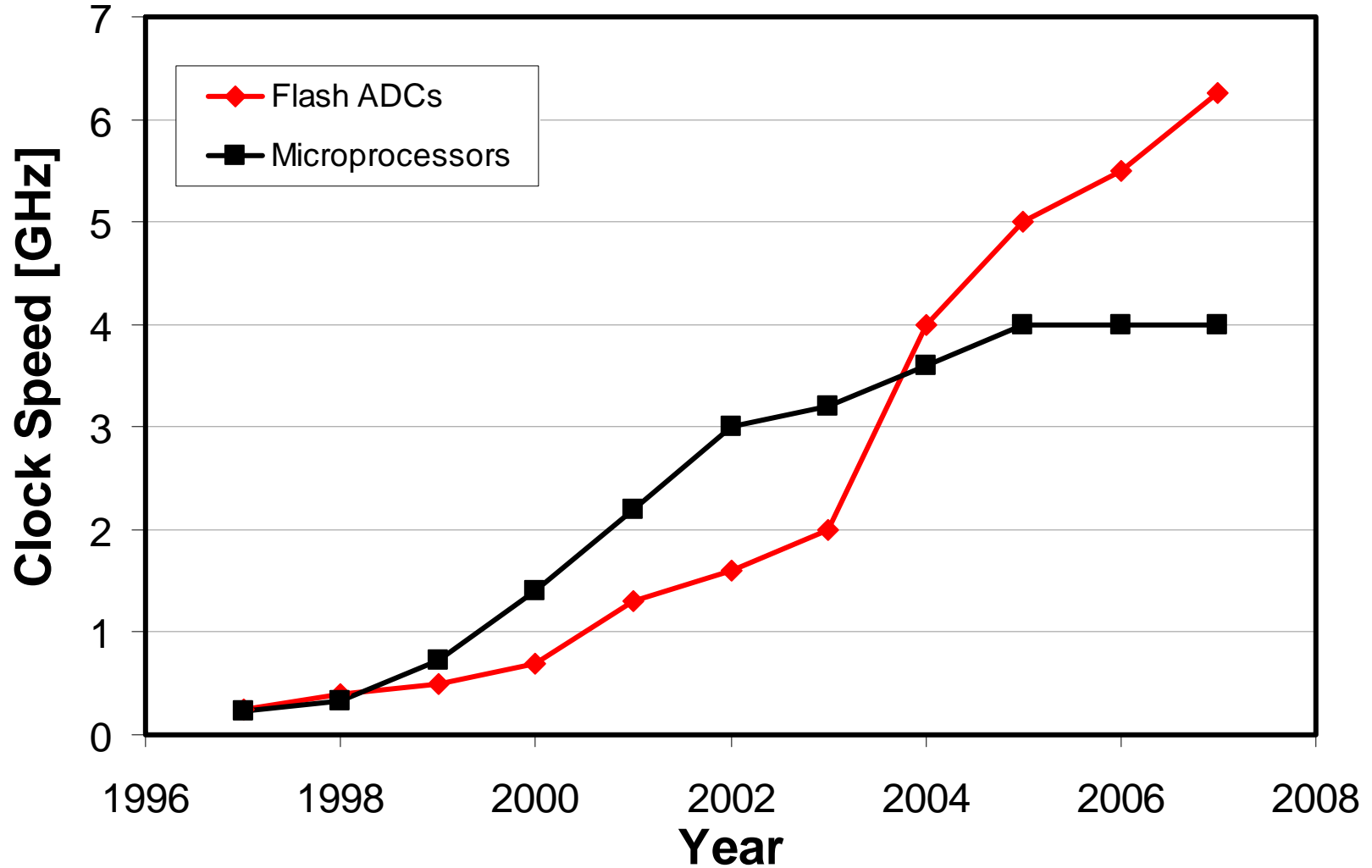
ISSCC 2006 / EVENING SESSION / E1

E1 Is the Digital Circuit Designer Dead?

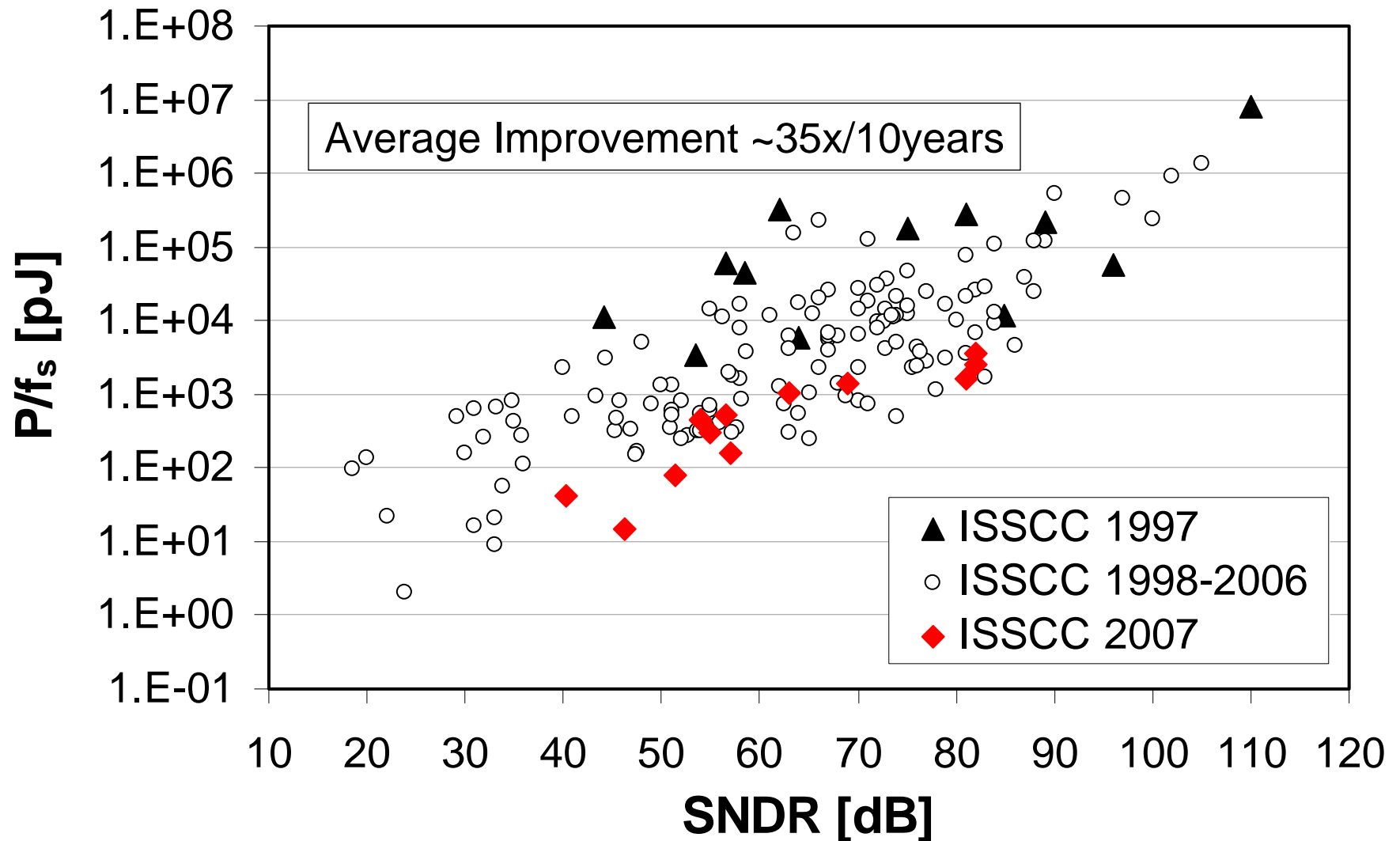
Organizer: Shannon Morton, Icera, Bristol, United Kingdom

Moderator: Dennis Fischette, AMD, Sunnyvale, CA

Flash ADC Speed



ADC Power Dissipation

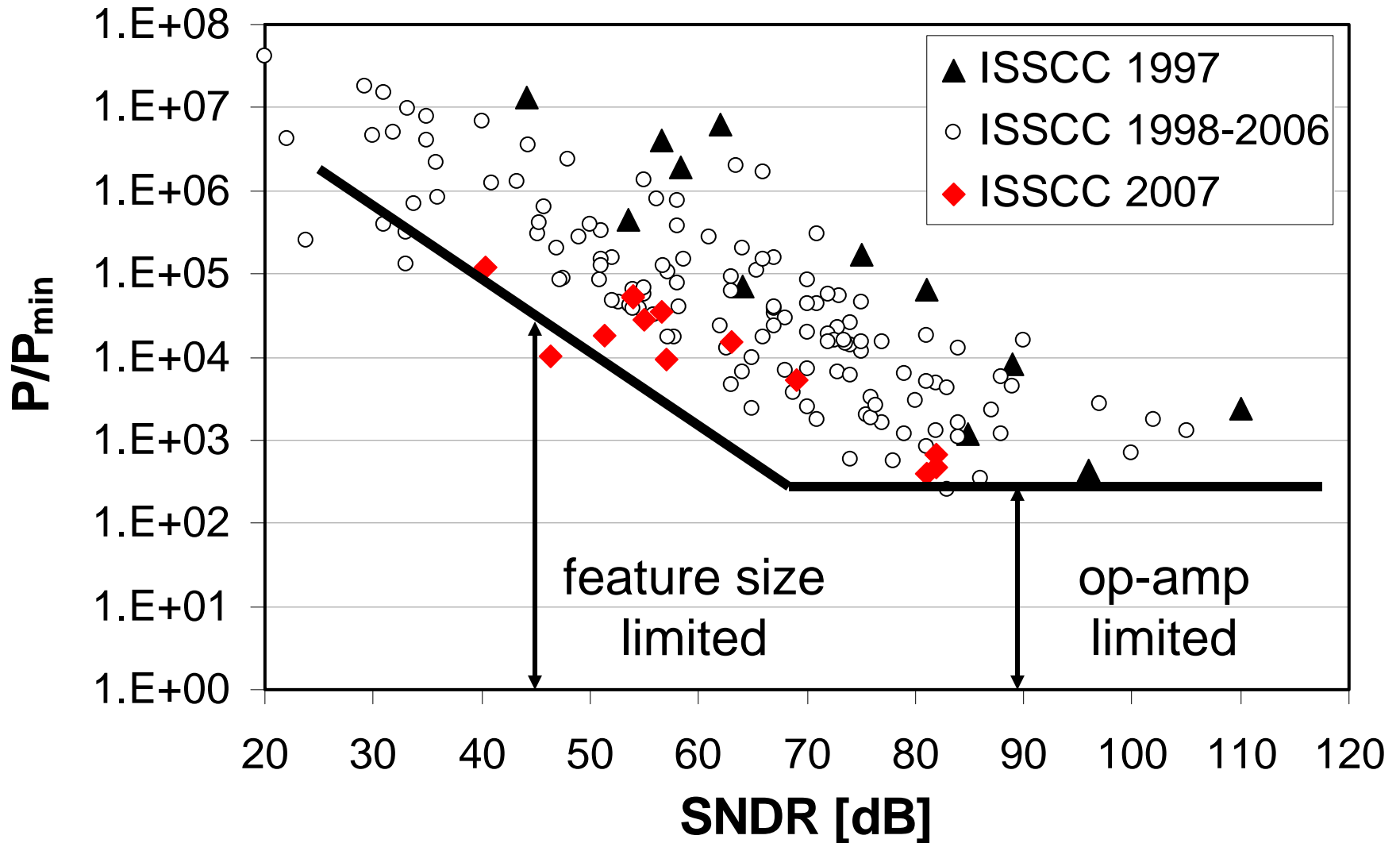


ADC Power Limit

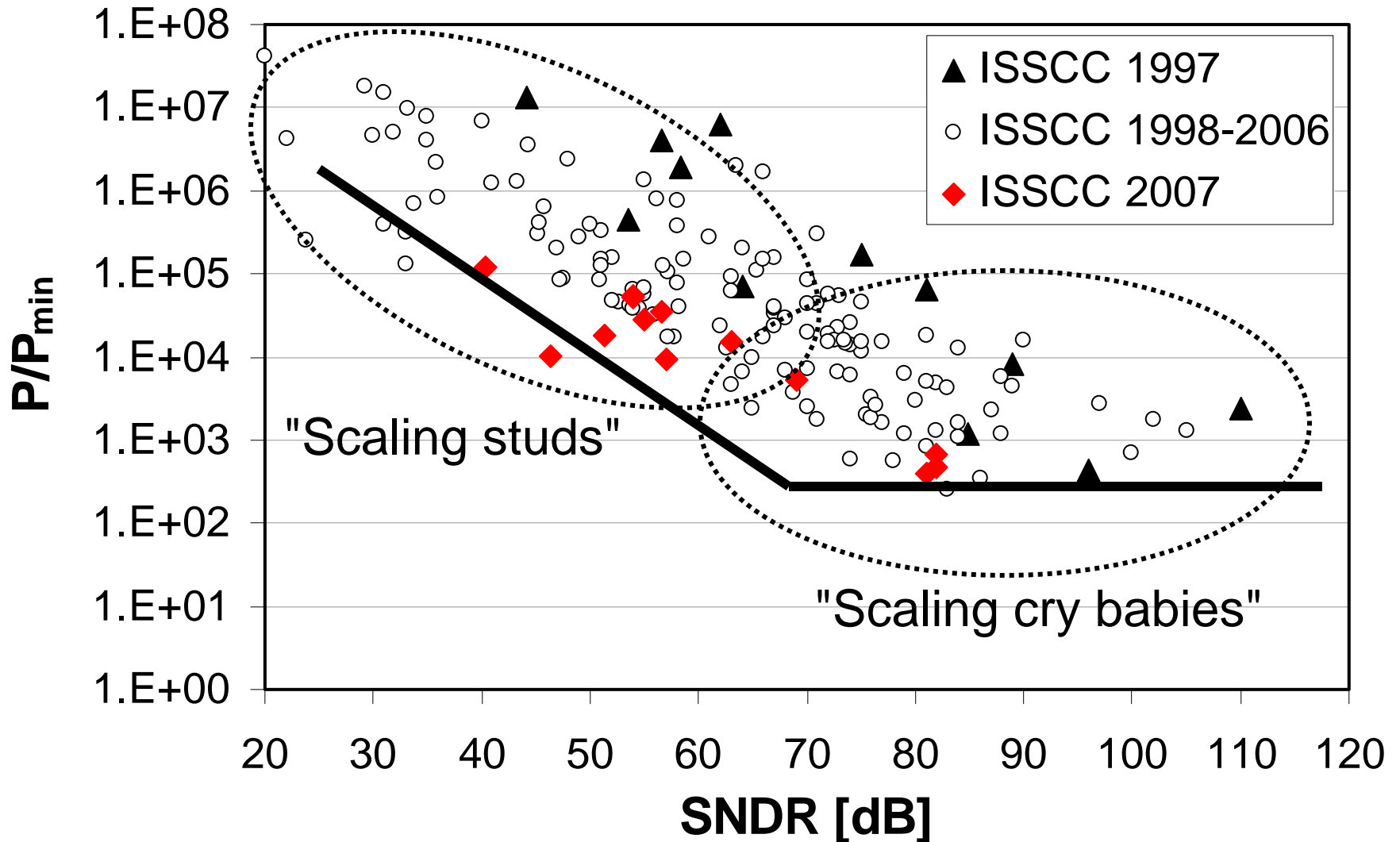
- Minimum power for sampled data A/D converter

$$P_{min} = 8 \cdot kT \cdot SNR \cdot f_s$$

Normalized ADC Power Dissipation



Normalized ADC Power Dissipation



"Scaling Studs"

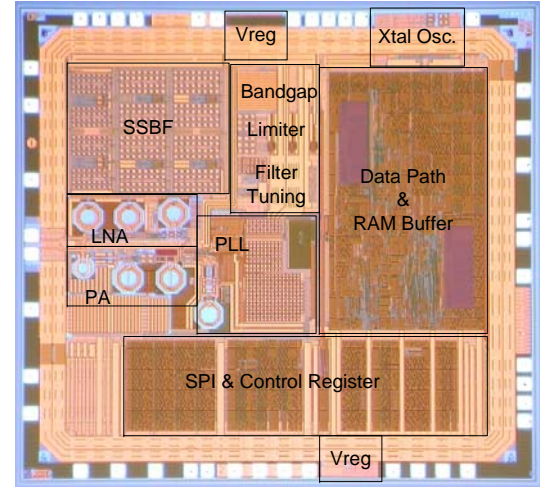
- Have never complained about scaling
 - Because they work on "<60dB" circuits
- Have achieved significant performance improvement over past few years, despite 1V supplies
- Life at 45nm and below
 - Will continue to benefit from scaling
 - By exploiting f_T and timing accuracy
 - Will use trim-DACs "everywhere" to overcome device mismatch

"Scaling Cry Babies"

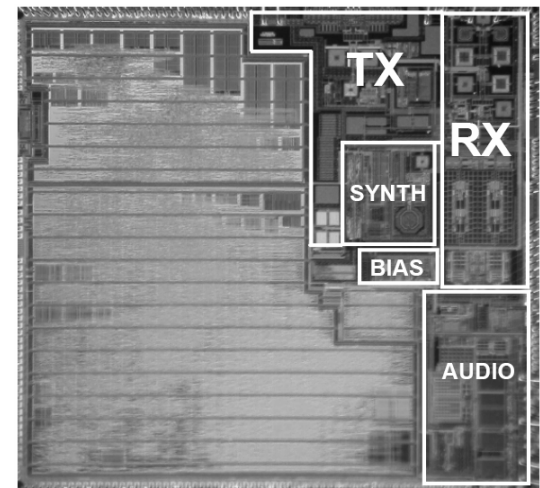
- Complain every time there is a reduction in supply voltage (5V, 3V, 2.5V, 1.8V, ...)
- Have to get used to trying "something new"
- Life at 45nm and below
 - Must try to get rid of complicated op-amps
 - Must leverage digital enhancement techniques
 - Must increasingly work with oversampling
 - Must carefully rethink if the system really needs high SNR...

The True Challenge

[Kluge, ISSCC 2006]



[Mehta, ISSCC 2006]



- Is system engineering!
- Can no longer "blindly" port analog to a new technology node
 - This doesn't even work for digital any more!
- Must rethink/improve system partitioning to leverage the strengths of nm technology
 - Transistor speed, transistor density, low energy computing

Lunch?

- At the end of the day, lunch at 45nm and below will be eaten by
 - Those who understand both analog & digital system design
 - Those who can justify the cost of these technologies

[Chang, ISSCC 2007]

