

KUNAL K. GHOSH

121 Campus Drive, Apt. #1313A
Stanford, CA 94305

(650) 353-1472
kghosh@stanford.edu

Education

Stanford University, Stanford, CA

Ph.D., Electrical Engineering

Expected June 2009

M.S., Electrical Engineering

June 2006

Research focus: instrumentation and systems for molecular imaging in living subjects, with an emphasis on optical imaging modalities, targeting applications in neuroscience and neurobiology.

University of Pennsylvania, Philadelphia, PA

The Jerome Fisher Program in Management and Technology

Dec 2003

The School of Engineering and Applied Sciences: B.S.E., Electrical Engineering (*summa cum laude*)

The Wharton School: B.S., concentration in Management (*summa cum laude*)

Honors and Awards

- 2004-2005 Stanford University Department of Electrical Engineering Fellowship
- 2004 Natural Sciences and Engineering Research Council of Canada (NSERC) Canada Graduate Scholarship
- 1999-2003 University of Pennsylvania Trustee Scholarship
- Dean's Lists, The School of Engineering and Applied Sciences and The Wharton School, 1999-2003
- Election to Tau Beta Pi Engineering honor society and Eta Kappa Nu Electrical Engineering honor society
- Best Student Paper finalist at 2003 IEEE International Symposium on Power Semiconductor Devices & ICs
- 1st in 2002-2003 University of Pennsylvania Electrical Engineering Senior Design Competition
- Great Eight finalist in 2003 Wharton Business Plan Competition (only Wharton undergraduate team in finals)
- 2002 Verizon Scholar
- 2001 Natural Sciences and Engineering Research Council of Canada (NSERC) Undergraduate Research Award
- Canadian Governor General's Academic Medal (99.3% high school graduating average), 1999

Research

Stanford University, Stanford, CA

Sept. 2004-Present

Research Assistant (Primary Advisor: Prof. Abbas El Gamal; Co-Advisor: Prof. Mark Schnitzer)

- *Integrated fluorescence microscopy for in vivo mammalian brain imaging*
Currently working on developing a fully-integrated and portable fluorescence microscopy system for *in vivo* brain imaging of anesthetized and freely-behaving mice. The system is expected to improve sensitivity and/or reduce the optical power at the specimen, enable imaging at higher speeds, and resolve feature sizes on the order of a few microns. The research is part of a joint collaboration with the laboratory of Prof. Mark Schnitzer, of the Departments of Biology and Applied Physics and the Stanford Bio-X Program.
- *Folded Multiple Capture: An architecture for high dynamic range, high speed image sensors*
Worked on the implementation of a new high dynamic range architecture, Folded Multiple Capture (FMC), targeted towards infrared (IR) imaging applications. A prototype implemented in a 0.18 μ m CMOS process achieved >138dB dynamic range at high speeds (1000 frames/sec) with high SNR (>60dB) and low power consumption (25.5nJ per pixel readout).
- *A per-pixel background subtraction scheme for imaging applications*
Involved in the implementation and validation of a per-pixel background subtraction scheme based on Pulse Frequency Modulation (PFM). The scheme is targeted for imaging applications that suffer from high background, for example, IR applications which often involve imaging scenes with small target signal variations over a large background offset, and non-invasive *in vivo* fluorescence imaging applications where the large background is due to tissue autofluorescence.

KUNAL K. GHOSH

University of Pennsylvania, Philadelphia, PA

Sept. 2002-April 2003

Senior Design Project (Advisors: Prof. Jan Van der Spiegel and Prof. Nader Engheta)

- *A CMOS image sensor with polarization difference imaging*
Polarization difference imaging (PDI) is a biologically-inspired technique that seeks to improve the visibility of objects in scattering media. The project was inspired by the quest to integrate a PDI system with a CMOS camera module. A prototype implemented in a 0.5um CMOS process demonstrated the proof-of-concept. A fully integrated imaging system has applications in nautical, aeronautical and space sensor systems, where imaging in harsh light scattering conditions is required. The project is still on-going at Penn as of early 2008.

University of Toronto, Toronto, Canada

May-August 2001

Visiting Research Associate (Advisor: Prof. C. André T. Salama)

- *A high voltage CMOS ADSL line driver*
Designed a high voltage ADSL line driver for short loop Subscriber Line Interface Circuits (SLICs). Implemented in a conventional 50V 0.8um CMOS process, the line driver exhibited significantly better performance than previous designs implemented in more complex and expensive BiCMOS processes.

Teaching

Stanford University, Stanford, CA

Winter 2007

Teaching Assistant, EE316: Advanced VLSI Devices (Prof. H. -S. Philip Wong)

- Held weekly office hours and review sessions as needed, helped in design of problems and solutions, grading

University of Pennsylvania, Philadelphia, PA

Spring 2003

Teaching Assistant, MGMT 237: Management of Technology (Prof. William F. Hamilton)

- Served as mentor to students (class exclusive to M&T students), helped in grading cases and research papers

University of Pennsylvania, Philadelphia, PA

Fall 2001

Teaching Assistant, EE 215: Electrical Circuits I (Prof. Nader Engheta)

- Held weekly office hours and review sessions as needed, helped in preparing solutions and grading

Professional Experience

Agere Systems (now LSI), Allentown, PA

May-August 2004

Technical Associate (Mass Storage Group)

- Investigated customer performance concerns related to analog front-end (AFE) blocks in hard disk-drive SoCs
- Identified root cause and addressed concerns through ATE and DTE testing, FIB procedures, and simulations
- Implemented necessary design changes and worked with customer team to ensure concern resolution

Angel investment activities, Toronto, Canada

January-March 2004

Analyst

- Worked closely with angel investor providing seed financing (< \$100K) to Toronto-based startups
- Assisted in business opportunity evaluations and hands-on consulting to founding teams at funded ventures
- Main objective was to learn and experience the investment and entrepreneurial dynamics in startups

McKinsey & Company, Toronto, Canada

June-August 2003

Summer Analyst

- Core team member on growth strategy engagement
- Led workstream on strategies for client to maintain leadership in an increasingly competitive market segment
- Closely interacted with team and client to formulate action plan and associated implementation strategy

KUNAL K. GHOSH

May-August 2002

Agere Systems (now LSI), Allentown, PA

Technical Associate (Mass Storage Group)

- Involved in the design of analog integrated circuits for hard disk drive controller and interface electronics
- Cornerstone project was the design of a 1 V bandgap reference circuit in a 1.2 V 0.13 μm CMOS process
- Design in production in Serial ATA hard disk-drive chipsets and adopted by other company business units

Activities and Diversions

- President, Bay Area Penn M&T Club, 2007-Present
- Penn Silicon Valley Secondary School Committee, 2006-Present
- Vice President, Membership, Wharton Club of Northern California, 2005
- Avid sailor with working knowledge of San Francisco Bay and Indian Ocean waters off the east coast of Africa

Publications

Refereed Journal Papers

- [J-1] J. Deng, K. Ghosh and H. -S. P. Wong, "Modeling Carbon Nanotube Sensors," IEEE Sensors Journal, vol. 7, no. 9, pp. 1356-1357, 2007.

Refereed Conference Papers

- [C-1] S. Kavusi, K. Ghosh and A. El Gamal, "A Per-Pixel Pulse-FM Background Subtraction Circuit with 175ppm Accuracy for Imaging Applications," 2007 IEEE International Solid-State Circuits Conference, pp. 504-505, San Francisco, CA, 11-15 February 2007.
- [C-2] S. Kavusi, K. Ghosh and A. El Gamal, "Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits," *invited*, 2006 IFIP 14th International Conference on Very Large Scale Integration, pp. 36-41, Nice, France, 16-18 October 2006.
- [C-3] S. Kavusi, K. Ghosh, K. Fife and A. El Gamal, "A 0.18 μm CMOS 1000 frames/sec, 138dB Dynamic Range Readout Circuit for 3D-IC IR Focal Plane Arrays," 2006 IEEE Custom Integrated Circuits Conference, pp. 229-232, San Jose, CA, 10-13 September 2006.
- [C-4] K. Ghosh and C. A. T. Salama, "A High Voltage CMOS ADSL Line Driver," 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, pp. 105-108, Cambridge, U.K., 14-17 April 2003.

Refereed Journal Papers in Preparation

- [J-2] S. Kavusi, K. Ghosh, K. Fife and A. El Gamal, "A 0.18 μm CMOS 1000 frames/sec, 138dB Dynamic Range Readout Circuit for 3D-IC IR Focal Plane Arrays," IEEE Sensors Journal.
- [J-3] S. Kavusi, K. Ghosh and A. El Gamal, "A Per-Pixel Pulse-FM Background Subtraction Circuit with 175ppm Accuracy for Imaging Applications," IEEE Journal of Solid-State Circuits.

Book Chapters

- [B-1] S.Kavusi, K.Ghosh and A. El Gamal, "Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits," *invited*, VLSI-SoC: Research Trends in VLSI and Systems on Chip, IFIP Series, vol. 249, Springer, 2007.

Selected Research Presentations

- [P-1] "Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits", EPFL (Swiss Federal Institute of Technology, Lausanne), October 20, 2006.
- [P-2] "A High Voltage CMOS ADSL Line Driver", Micronet R&D Workshop, Toronto, Canada, October 2003.
- [P-3] "CMOS Camera-on-Chip with Polarization Difference Imaging", University of Pennsylvania, April 2003.