DSP-Free Coherent Receivers for Data Center Links

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Abstract: We review low-power DSP-free coherent receiver architectures for DP-QPSK that exhibit performance comparable to their DSP-based counterparts, while consuming an estimated ~ 4 W for 200 Gbit/s DP-QPSK in 90-nm CMOS.

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1. Introduction

The IEEE 802.3bs task force has recently adopted 4-PAM to enable bit rates of 50 and 100 Gbit/s per wavelength in data center links. However, 4-PAM systems already face tight implementation constraints that will hamper their scalability in the long term. For instance, 50 Gbit/s 4-PAM links for inter-data center applications, i.e., amplified links near 1550 nm reaching up to 80 km, require optical signal-to-noise ratio (OSNR) greater than 29 dB [1]. 100 Gbit/s 4-PAM links for intra-data center applications, i.e., unamplified links near 1310 nm reaching up to ~ 10 km, have limited power margin, as their receiver sensitivity is only -7 dBm [2]. The receiver sensitivity may be improved by 4.5 dB using avalanche photodiodes or by 6 dB using semiconductor optical amplifiers [3].

Alternative techniques based on single-sideband discrete-multitone or Stokes vector detection [4] are spectrally efficient, but they rely on power-hungry analog-to-digital converters (ADCs) and digital signal processing (DSP) and do not address the problems of high required OSNR or limited power margin. Coherent detection solves these problems, but conventional DSP-based coherent receivers designed for long-haul transmission, which prioritize performance and reach, are suboptimal for data center applications, where cost, power consumption, and port density are paramount. These different design priorities may favor low-power architectures based on analog signal processing that avoid high-speed ADCs and DSP altogether.

In this paper, we summarize the results from [5], where we proposed homodyne DSP-free coherent receiver architectures for DP-QPSK. We show that for small chromatic dispersion (CD), the DSP-free receivers achieve performance comparable to their DSP-based counterparts, while the power consumption of the high-speed analog electronics for the most power-hungry architecture is expected to be approximately 4 W in 90-nm CMOS.

2. Homodyne DP-QPSK Receiver

Fig. 1 shows the proposed implementation of a DSP-free coherent receiver [5]. Polarization demultiplexing is performed by optical phase shifters that are controlled by low-speed circuitry (< 100 kHz). Other receiver operations such as carrier recovery, timing recovery, and symbol detection are performed in the high-speed analog electronics stage. Timing recovery and detection may be realized using conventional clock and data recovery (CDR); thus, we do not discuss them further herein.

2.1. Polarization Recovery

In short-reach links, polarization dependent loss (PDL) and polarization-mode dispersion (PMD) are negligible, hence the receiver only needs to recover the transmitted state of polarization by compensating for fiber-induced polarization rotation. This polarization rotation varies on a time scale of the order of milliseconds [5], allowing tracking with low-speed circuitry.

The polarization controller (inset of Fig. 1) consists of three cascaded phase shifter pairs. This configuration can perform any arbitrary polarization rotation [5, Appendix 1]. The relative phase shift through each phase shifter is adjusted by marker tone detection at baseband, as follows: at the transmitter, a low-frequency (< 50 kHz) marker tone is added, for instance, to the XI tributary. At the receiver, the phase shifters are adjusted to minimize the marker tone's presence in the XQ, YI, and YQ tributaries, so that the polarization rotation through the fiber is compensated.

Implementation of the phase shifters can be done using silica, lithium niobate, or any other material that has low loss and allows integration of a sequence of phase shifters. The phase shifters and waveguides do not need to support two polarizations. Endless polarization control can be achieved by cascading more phase shifting sections or resetting the phase shifters when one of them is close to its excursion limits. Resetting will cause burst errors during the switching period, but phase shifting speeds on the order of 1 ns for π phase shift, typical of phase shifters used for high-speed data modulation, ensure that burst errors can be corrected by 7% forward error correction (FEC) code at 56 Gbaud with standard interleaving depth (ITU-T G.709, 2016).

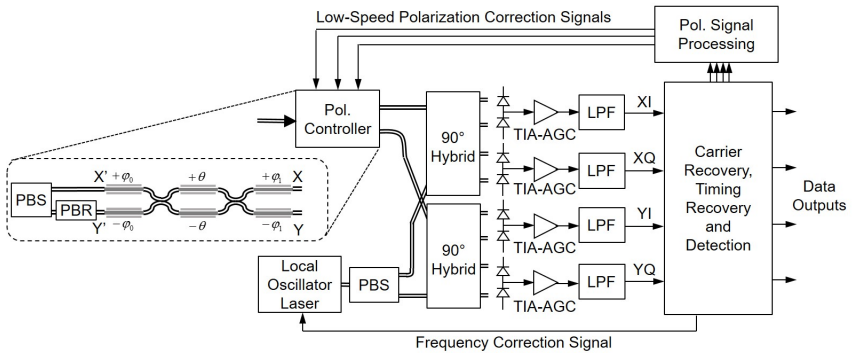

Fig. 1: Block diagram of coherent receiver architectures based on analog signal processing. Carrier recovery is detailed in Fig. 2. Acronyms: polarization beam splitter (PBS), polarization beam rotator (PBR), transimpedance amplifier (TIA), automatic gain control (AGC), low-pass filter (LPF).

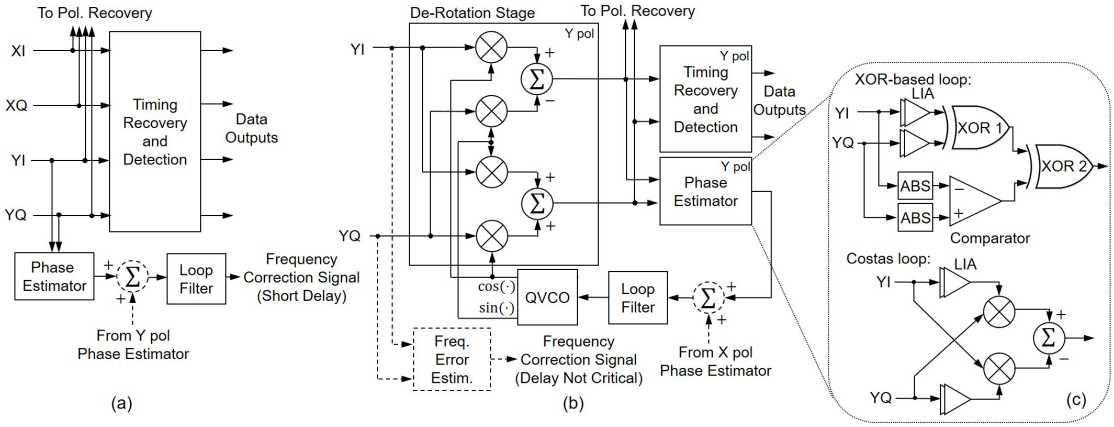

Fig. 2: Block diagrams of carrier recovery based on (a) OPLL and (b) EPLL (shown for one polarization only). The phase estimator is detailed in (c). Blocks in dashed lines denote optional implementations. Acronyms: limiting amplifier (LIA), full-wave rectifier (ABS), quadrature VCO (QVCO).

2.2. *Carrier Recovery*

Carrier recovery (CR) is performed by a phase-locked loop (PLL). A PLL consists of essentially three stages: phase estimator, loop filter, and oscillator. The oscillator is the local oscillator (LO) laser in an optical PLL (OPLL), and an electronic voltage-controlled oscillator (VCO) in an electrical PLL (EPLL). These similarities allow analysis of OPLLs and EPLLs under the same framework. The phase estimator stage wipes off the modulated data in order to estimate the phase error, which is then filtered by the loop filter, producing a control signal for the oscillator frequency that counteracts the random phase fluctuations due to phase noise.

The high-speed analog electronics stage is detailed in Fig. 2 for an OPLL and an EPLL. In an OPLL (Fig. 2a), the LO laser is frequency-modulated by the frequency correction signal generated by the CR stage. Hence, an OPLL requires an LO laser with wideband frequency modulation (FM) response and short propagation delay in the LO path to minimize the overall loop delay. Minimizing the loop delay requires substantial integration, since the loop includes the LO laser, hybrid, photodiodes, and all the subsequent electronics, which may not all be realized within a single chip. Notably, Park et al have demonstrated loop delays of only 120 ps for a highly integrated 40 Gbit/s binary PSK coherent receiver [6]. An EPLL (Fig. 2b) implementation eliminates requirements on LO laser FM response and on propagation delay at the cost of more complex analog electronics. Specifically, an EPLL requires a single-side band mixer in each polarization to de-rotate the incoming signals (see Fig. 2b), since the transmitter and LO lasers are not phase locked. Additionally, the frequency offset between the transmitter and LO lasers must always be within the lock-in and hold-in ranges of the EPLL, which are practically limited by the VCO frequency range (typically up to 10 GHz). This constraint can be satisfied by strict laser temperature control, or by a frequency error estimation stage based on a simple frequency discriminator to keep the LO laser frequency sufficiently close to the transmitter laser. Fig. 2c shows two possible implementations of a phase estimator for QPSK inputs. A conventional Costas loop requires two linear and wideband analog multipliers per polarization. We propose a novel multiplier-free phase detector based on XOR gates. Using simple operations, our proposed phase detector estimates the sign of the phase error rather than its actual value. The loop natural frequency is chosen to minimize the variance of the phase error. This optimization is realized by using a small-angle approximation to linearize the PLL equivalent control loop. The loop natural frequency varies for

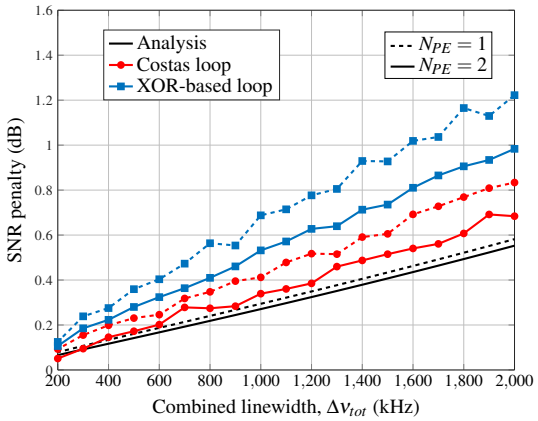

Fig. 3: SNR penalty vs combined linewidth for Costas loop and XOR-based loop for 200 Gbit/s DP-QPSK. Monte-Carlo simulation curves include thermal noise and ISI penalties, while analysis curves do not. N_{PE} is the number of polarizations used in phase estimation.

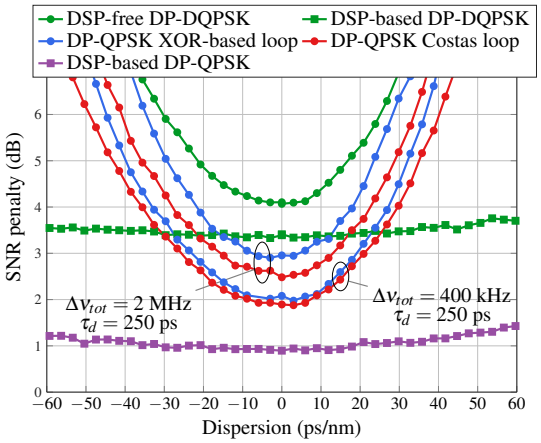

Fig. 4: SNR penalty versus dispersion for several receiver architectures. The x-axis represents total CD in intra-data center links or the residual CD after optical CD compensation in inter-data center links. $\Delta\nu_{tot}$ is the sum of the transmitter and LO lasers linewidth, and τ_d is the PLL loop delay. $\Delta\nu_{tot} = 400$ kHz and $\tau_d = 250$ ps, when not specified.

each case, but is typically about 110 MHz. Fig. 3 shows that the XOR phase detector exhibits minimal penalty relative to a traditional Costas loop. Fig. 3 also shows that there is minimal penalty by using only one of the polarizations to estimate the phase error.

3. Performance comparison

Fig. 4 compares the proposed DSP-free architectures with their DSP-based counterparts at 224 Gbit/s in terms of the SNR penalty with respect to a reference system, which is an ideal additive white Gaussian noise channel, where the target BER of 1.8×10^{-4} is achieved with SNR ≈ 11 dB (OSNR ≈ 16 dB). Note that a 1-dB SNR penalty corresponds to a 1-dB OSNR penalty. Fig. 4 also shows results for DP-differential QPSK (DQPSK) systems, for which CR is not necessary, since information is encoded in the phase difference between two consecutive symbols [5].

At small CD, DSP-free systems exhibit 1 dB SNR penalty compared to their DSP-based counterparts due to intersymbol interference (ISI) and suboptimal receiver filtering, which in our simulations is a 5th-order Bessel filter with bandwidth equal to 70% of the symbol rate. The SNR penalty of DSP-free reaches 5 dB at roughly 35 ps/nm. XOR-based loop exhibits minimal penalty compared to Costas loop, even when the total linewidth is 2 MHz. OPLL and EPLL differ in terms of total linewidth and loop delay. An OPLL-based receiver requires tunable lasers, which exhibit linewidths > 1 MHz, while EPLL-based receivers can use off-the-shelf lasers with linewidths on the order of 200 kHz. In this comparison, we assumed $\tau_d = 250$ ps although the loop delay is negligible in an EPLL.

Assuming realistic receiver losses and a 5-dB SNR penalty due to ± 35 ps/nm dispersion, the receiver sensitivity becomes -26.5 dBm, which is nearly 13 dB better than that of an amplified 4-PAM system at half the bit rate. This sensitivity would allow eye-safe systems near 1310 nm to achieve a reach up to 40 km. In fact, eye-safe systems with 100 GHz wavelength spacing could support 49 channels with 5 dB of margin, and systems with 200 GHz wavelength spacing could support 25 channels with 8 dB of margin. The power consumption comparison is detailed in [5]. While the DSP and ADCs of a DSP-based receiver for 56 Gbaud DP-QPSK optimized for short reach is expected to consume 30 W in 28-nm CMOS, the high-speed analog electronics of an EPLL-based DSP-free receiver is conservatively estimated to consume roughly 4 W in 90-nm CMOS.

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