SUKRU BURC ERYILMAZ

CONTACT INFORMATION

Address: B113X Center for Integrated Systems Paul G. Allen Building 420 Via Palou Mall MS 4070 Stanford, CA 94305
Email: eryilmaz@stanford.edu

EDUCATION

PhD Candidate, **Stanford University** *2011 – 2017*
PhD Major: Electrical Engineering, **PhD Minor:** Computer Science
Advisors: Prof. H.-S. Philip Wong (Stanford) / Prof. Gert Cauwenberghs (UCSD)
Thesis: Brain-inspired and non-conventional computing with emerging memory devices

MS, Electrical Engineering**, Stanford University** *2011 – 2013*

BS, Electrical and Electronics Engineering *2007 – 2011*
Bilkent University, Ankara, Turkey

FIELDS OF INTEREST

Neuromorphic hardware design, Emerging non-volatile-memory design/characterization/ modeling, Computer Architecture, Machine learning.

INDUSTRY EXPERIENCE

- **Micron Technology (Summer 2013)-*Emerging Nonvolatile Memory Intern:*** Non-volatile memory electrical/statistical characterization, electro-thermal modeling, write disturb modeling. ***Manager: Dr. Bob Gleixner***
- **Engineers Gate (Summer 2015)-*Quantitative Research Intern:*** Evaluating/optimizing machine learning algorithms on finance data, instruction level code optimization. ***Manager: Dr. Stephen Owen***

COURSEWORK

Advanced Multicore Systems (CS316), Computer Systems Architecture (EE282), Program Analysis and Optimization (CS243), Mining Massive Datasets(CS246), Nanoelectronics (EE316), Digital CMOS Integrated Circuits (EE313), Fundamentals of Analog IC Design (EE214), Machine Learning (CS229), Probabilistic Graphical Models (CS228), Convex Optimization (EE364)

RESEARCH EXPERIENCE

Center for Integrated Systems, Stanford University

- ***Microarchitectural techniques to improve lifetime of 3D RAM based on emerging non-volatile memory technology*.** Data steering algorithms for memory writes: zsim/PIN/NVSim tools are being used. Coadvisers: Subhasish Mitra/Heiner Litz
- ***Design/test of a neuromorphic chip (28 nm) with monolithically integrated non-volatile memory:*** I taped out CMOS neural network chip with digital asynchronous communication. Monolithic RRAM integration is done. ***Advisor: Prof. H.-S. Philip Wong/Prof. Gert Cauwenberghs (UCSD)***
- ***Demonstration of supervised and unsupervised learning on neuromorphic hardware that uses single nanoscale multilevel memory cell as synaptic element:*** I demonstrated pattern recognition with Hopfield network and Restricted Boltzmann Machine using nanoscale phase change memory devices, and performed variation/energy consumption analysis. ***Advisor: Prof. H.-S. Philip Wong***
- ***Statistical modeling of analog-resistive-switching behavior in emerging nonvolatile memory devices. Advisor: Prof. H.-S. Philip Wong***
- ***Novel electrode/heater structures for reduced energy consumpton in PCM(Phase change memory)***: We deposited multilayer stacks by sputtering and measured the thermal and electrical properties for PCM electrode applications. ***Advisor: Prof. Mehdi Asheghi***

Massachusetts Institute of Technology, Research Laboratory of Electronics,
Advisors: Prof. Mehmet Fatih Yanik, *June-Sept. 2010*
Two Photon Laser Scanning Microscopy for Brain Cell Imaging: We constructed a **two photon laser scanning microscope** for neuron imaging and neuronal surgery.

UNAM (Institute for Materials Science and Nanotechnology), Bilkent University,
Advisor: Prof. Ali Kemal Okyay *2009-2011*

- ***Nanocrystal Hybridized LEDs and Solar Cells*:** Demonstration of white light generation through wavelength conversion using Silicon nanocrystals
- ***Plasmonics Enhanced Infrared Photodetectors:*** Increasing sensitivity of Ge-on-Si MSM photodetectors using plasmonic nanostructures.

MAJOR PUBLICATIONS

Book Chapters:

- Rakesh Jeyasingh, Ethan Ahn, **Sukru Burc Eryilmaz**, Scott Fong, H. S. Philip Wong, Chapter 5: Phase Change Memory, Emerging Nanoelectronic Devices, Wiley Publishing, UK, in press.

Peer-reviewed articles:

- **S. B. Eryilmaz**, D. Kuzum, R. J. D. Jeyasingh, S. Kim, M. Brightsky, C. Lam, H.-S. Philip Wong, "Brain-like associative learning using a nanoscale non-volatile phase change synaptic device array," *Frontiers in Neuroscience*, 8, 205 (2014).
- **S. B. Eryilmaz**, O. Tidin, A. K. Okyay, "Plasmonic Nanoslit Array Enhanced Metal-Semiconductor-Metal Optical Detectors," *IEEE Photon. Technol. Lett,* vol. 24, no. 7, pp 548-550, April 2012.
- **S. B. Eryilmaz**, O. Tidin, A. Yesilyurt, and A. K. Okyay, "Silicon Nanocrystal Hybridized Visible LEDs: A Low Cost Path for Global Lighting," *International Journal of Material Science and Electronics Research***,** January (2011).

Conference Papers:

- **S. B. Eryilmaz,** S. Joshi, E. Neftci, W. Wan, G. Cauwenberghs, H.-S. P. Wong, "Neuromorphic architectures with electronic synapses," **invited paper for Cognitive Computing Hardware Session, ISQED 2016.**
- **S. B. Eryilmaz,** D. Kuzum, S. Yu, H.-S. P. Wong, "Brain inspired computing with emerging memories," **invited paper, IEDM 2015.**
- J. H. Engel**, S. B. Eryilmaz**, S. Kim, M. BrightSky, C. Lam, H.L. Lung, B. Olshausen, H.-S. Philip Wong, "Capacity optimization of emerging memories: A Shannon-inspired approach to device characterization," accepted to **IEDM 2014.**
- **S. B. Eryilmaz**, D. Kuzum, R. J. D. Jeyasingh, S. Kim, M. Brightsky, C. Lam, H.-S. Philip Wong, "Experimental Demonstration of Array Level Learning in Phase Change Synaptic Devices," p 25.5.1-4, **IEDM 2013.**
- A. Sood, **S. B. Eryilmaz**, R. Jeyasingh, J. Cho, M. Asheghi, H.-S. P. Wong and K.Goodson," Thermal characterization of multilayered TiN/TaN films for electrodes in phase change memory," **IEEE ITHERM 2014**
- **S. B. Eryilmaz,** and A. K. Okyay, "Plasmonic Nanoslit Enhanced Metal-Semiconductor-Metal Optical Detectors," *OSA FiO*, San Jose, CA, Oct 16-20, 2011.
- **S. B. Eryilmaz**, O. Tidin, A. Yesilyurt, and A. K. Okyay, "Silicon Nanocrystal Hybridized Visible LEDs: A Low Cost Path for Global Lighting," *NanoTr 6*, Cesme, Turkey, Jun 15-18, 2010.

Invited Talks:

- "Analog-non-volatile-memory based spiking neuromorphic systems for online learning", Cognitive Computing Hardware Special Session, **ISQED, 2016**.
- "Approaching the problem of financial forecasting from machine learning persective", **Bay Area Quant Club organized by Quantiacs, LLC**, 2015.
- "Bio-inspired Computing Machines with Emerging Memory Devices", **Intel Labs, Santa Clara**, 2015.
- S. Joshi*, **S. B. Eryilmaz***, G. Cauwenberghs, H.-S. P. Wong, "Mapping Vision Algorithms on a Neuromorphic Array Architecture," **IEEE/ACM International Conference on Computer Aided Design (ICCAD)**, San Jose, CA, paper 2B.2, November 2-6, 2014. (Special session: Design, Modeling and Tools for Video Analytics Using Emerging Devices) (*:Joint talk)
- **S. B. Eryilmaz**, "Cognitive Computing Using Nanoscale Electronic Synapses: Merging Nanoelectronics and Neuroscience", **Lockheed Martin Palo Alto Colloquia**, April 18, 2013.

Non peer-reviewed articles and technical reports:

- S. O. Arik, **S. B. Eryilmaz**, A. Goldberg, "Supervised classification based stock prediction and portfolio optimization," arXiv:1406.0824 [q-fin.ST].

TEACHING ACTIVITIES

Course assistant to EE316-Advanced VLSI Devices-given by Prof. Philip Wong at Stanford: Devised and organized homeworks, exams, and final TCAD simulation project; held office hours and individual meetings per request to help students

CURRICULAR PROJECTS

- **Microarchitectural techniques to improve the system lifetime of hybrid main memory based on STT-MRAM and RRAM. (**Advanced Multicore Systems/ **Dr. Heiner Litz.)**
- **Design of datacenter hardware and software** using BigHouse simulator; **analyzing tradeoffs of multicore architectures** using zsim simulator (Computer Systems Architecture class; **Prof. Christos Kozyrakis**).
- **Portfolio optimization using supervised learning and convex optimization:** We used support vector machines and dimension reduction techniques (Principal component analysis) and on thousands of securities' data for stock picking and portfolio optimization. (Machine Learning class, **Prof. Andrew Ng)**
- **SRAM Design-** SRAM Array, Timing generators, Low power SRAM design. Simulations are performed using Hspice and Cadence**.**
- **Review of 3D NAND Flash Memory Technology:** Challenges and Future Directions
- **FD-SOI MOSFET Parasitics Engineering** using TCAD simulation tools (Sentaurus)
- **Design of an Optical Sensor Amplifier Circuit (Prof. Robert Dutton):** An amplifier circuit with several stages was designed using Hspice software (2011)

AWARDS & HONORS

- 2nd place in Quantiacs kickoff algorithmic trading competition (1-year Sharpe Ratio of 1.2 with a 1-year return of 13.8%) *2015*
- John Bardeen Student Research Award for Excellence in Nanodevices Research- 2014 SONIC Annual Meeting *2014*
- Selected to Marquis Who's Who in the World *2014-2015*
- The Eltoukhy Family fellowship from Department of Electrical Engineering-Stanford University (1 year full tuition and stipend) *2011-2012*
- Ranked top 20 **%** in the world in the IEEExtreme programming competition with Java. *2009*
- Scholarship of Prime Ministry for undergraduate education *2007-2011*
- 5 Gold, 2 Silver and 2 Bronze medals in Mathematical Olympiads organized by The Scientific and Technological Research Council of Turkey (TUBITAK) and other institutions *2003-2007*

COMPUTER SKILLS

Programming Languages: Java, Verilog, C, C++, MATLAB, Python
Applications: TCAD (Sentaurus, Lumerical**),** Labview, Cadence Virtuoso, Hspice, BigHouse, zsim.

PROFFESIONAL ACTIVITIES

Ad-hoc reviewer for:

- IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- Frontiers in Neuroscience-Neuromorphic Engineering

EXTRA-CURRICULAR

- Served as the financial officer of Stanford Turkish Association for 2 years (2013-15)
- Served as the financial officer of Stanford Windsurfing Club for 2 years (2014-16)

REFERENCES

- **Prof. H.-S. Philip Wong**, *Stanford University*
- **Prof. Gert Cauwenberghs,** *UCSD*
- **Dr. Stephen Owen,** *Engineers Gate (previously Morgan Stanley)*
- **Dr. Chung Lam,** *IBM Research*
- **Dr. Robert Gleixner**, *Micron Technology, Inc.*
- **Prof. Mehmet Fatih Yanik**, *Research Lab of Electronics, MIT*
- **Prof. Ali Kemal Okyay**, *Bilkent University*, Turkey