

# A 25 $\mu$ W Differential Track-and-Hold Circuit

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**Abstract**—A Track-and-Hold circuit was designed for a 0.18 $\mu$ m process and performance was characterized using Hspice simulations. An open loop, source-follower architecture was chosen over the more commonplace bottom-plate sampling architecture in order to eliminate the power requirements of an OTA. In this technology, adequate transistor performance can be obtained even in the subthreshold region where benefits arise from low noise and low power operation. The circuit consumes 25  $\mu$ W with a SNDR of 86dB at 100 kS/s and occupies roughly 0.1mm<sup>2</sup> of chip area.

## I. INTRODUCTION

OVER the past several decades, improvements in transistor speed that accompany newer technologies have enabled faster and faster analog-to-digital converters (ADCs)[1]. However, in the race to build the fastest converters, it is easy to overlook opportunities to improve along other dimensions. Specifically, low-power converters can be realized by exploiting two basic trends in technology scaling. First, newer technologies yield physically smaller circuits, which inherently have less parasitic capacitance. This allows smaller signal currents to be used. Additionally, due to increasing  $f_T$ , moderate transistor speeds can be obtained even when operated at very small currents, even down into the subthreshold (weak inversion) region. In weak inversion, MOSFETs are known to behave similar to BJTs and thereby achieve better noise performance. In this design, we leverage these trends to develop a track-and-hold circuit intended for use in low-speed, moderate-resolution ADCs.

The overall goal of the design is to maximize a figure of merit (FOM) given by

$$\text{FOM} = \frac{f_s \cdot \text{SNDR}_{\text{Power}}}{P_{\text{ckt}} + P_{\text{drive}}} \quad (1)$$

where

$$P_{\text{drive}} = 6 \cdot V_{\text{dd}} \cdot 2\pi \cdot \frac{f_s}{2} \cdot C_{\text{in}} \cdot V_{\text{in}} \quad (2)$$

$f_s$  is the sampling frequency,  $\text{SNDR}_{\text{Power}}$  is the ratio of signal power to noise plus distortion power,  $P_{\text{ckt}}$  is the average power consumed by the circuit,  $V_{\text{dd}}$  is the supply voltage,

$C_{\text{in}}$  is the input capacitance, and  $V_{\text{in}}$  is the maximum amplitude of a single ended input signal.

Note that this is a different FOM than the familiar one given by Walden in [2]. Walden's FOM remains constant if each added bit of resolution accompanies a 2X increase in power consumption. This new FOM remains constant if each added bit of resolution accompanies a 4X increase in power consumption. It has been shown in [3] that, once a circuit becomes noise limited, it requires a 4X increase in power for a 2X increase in resolution. Therefore this new FOM is preferred for noise limited designs because it relates power and noise on a fundamental level. In effect, it specifically removes a "loophole" in the Walden FOM that rewards very high speed designs.

A half circuit of our final design is pictured in Fig. 1. Although [4] uses a similar architecture for very high speed designs, we believe that it can achieve a high FOM at low frequencies because it operates well within the capabilities of the technology and because it requires very little bias current. It also compares very favorably with [5], which, on a similar power budget, only achieves 65 dB SNDR. Our design consists of an NMOS switch, a hold capacitor and a single-transistor PMOS buffer. Additionally, clock boosting is used on the input switch to reduce the signal dependence of charge injection as well as signal-dependent switch resistance modulation [6].

There are two main reasons why designers may be suspicious of this type of circuit. First, it is generally assumed that voltage followers do not yield distortion performance at the level of an OTA. Secondly, the architecture does not accommodate bottom plate sampling, leaving the door open for signal dependent charge injection. Both of these issues will be addressed in this report.

On the other hand, there are several reasons why such an architecture has practical appeal. First of all, it is an efficient use of both power and silicon area: the largest consumers of both are in fact the sampling and load capacitors. Intuitively, this suggests that the device is operating very efficiently since little energy is wasted on parasitics. One potential drawback is that this circuit tries to manage noise in a very brute force manner – by increasing capacitance. If die area were overly critical, then an oversampling architecture may seem more attractive because of the ability to trade noise for bandwidth (rather than for die area). But there are many applications where oversampling latencies are detrimental and this type of sampling is preferred. In low-frequency applications where ADC latency is performance-prohibitive, this circuit topology is extremely attractive.

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## II. DESIGN

### A. Noise Considerations

Generally speaking, an optimized analog circuit should be noise-limited if it is to be power efficient; otherwise power can be saved by reducing capacitances and the operating currents required to drive them. Using this rule of thumb, desired noise performance can be used to estimate required capacitances early in the design process, following a simple noise analysis. Fig. 2 suggests a straightforward two-stage noise analysis procedure for our open loop sample and hold circuit. According to the equipartition theorem, any sampling circuit that can be modeled like the ‘‘First stage noise’’ portion of the drawing will contribute hold-mode uncertainty equal to  $kT/C_s$ . Therefore we can write:

$$V_{n1}^2 = \frac{kT}{C_s} \quad (3)$$

There is also the possibility for additional hold-mode uncertainty due to signal-independent variations in the charge injected onto  $C_s$  during the sampling instant by switch feedthrough (signal-dependent variations will, in general, cause gain, offset, or HD errors whereas signal-independent errors can be interpreted as noise. Note that although such noise is by definition uncorrelated with the input signal, it is not necessarily random or white). However, it is assumed that signal-dependent variations will be stronger than signal-independent ones, and therefore feedthrough noise is considered negligible by virtue of the SFDR spec.

Assuming the load resistance is dominated by  $1/g_{m2}$ , the second stage can be redrawn as shown in Fig. 3 for noise analysis. Because the bias network contributes common mode noise, there are only two noise sources to consider at the output node, one due to  $M2$  and one due to the load (note that the  $1/g_{m2}$  resistance is noiseless in this case). First consider noise from  $M2$ . Because this circuit operates with very small currents,  $M2$  operates in the subthreshold region with a very small  $V_{gs}$ . As shown in [7], a MOSFET operating in subthreshold behaves similar to a BJT transistor. This yields two possibilities for noise calculations, depending on which interpretation is given to the region of operation. Specifically, the following equations are given for noise current in both BJT and FET transistors

$$\text{(BJT)} \quad i_c^2 = 2q \cdot I_C \cdot \Delta f \rightarrow I_C = gm \cdot \left( \frac{n \cdot kT}{q} \right) \rightarrow i_c^2 = 2 \cdot n \cdot kT \cdot gm \cdot \Delta f \quad (4)$$

$$\text{(FET)} \quad i_d^2 = 4kT \cdot \gamma \cdot gm \cdot \Delta f \quad (5)$$

where  $n$  is typically 1.5 and  $\gamma$  is typically 1, though it is a strong function of  $V_{gs}$  [8]. Using Fig. 3, it is straightforward to derive total integrated noise using either model.

$$\text{(BJT)} \quad v_{n2}^2 = (2 \cdot n \cdot kT \cdot gm) \cdot \left( \frac{1}{gm^2} \right) \cdot \left( \frac{1}{2 \cdot \pi \cdot C_L \cdot \frac{1}{gm}} \cdot \frac{\pi}{2} \right) = \frac{n \cdot kT}{2C_L} \quad (6)$$

$$\text{(FET)} \quad v_{n2}^2 = (4 \cdot \gamma \cdot kT \cdot gm) \cdot \left( \frac{1}{gm^2} \right) \cdot \left( \frac{1}{2 \cdot \pi \cdot C_L \cdot \frac{1}{gm}} \cdot \frac{\pi}{2} \right) = \frac{\gamma \cdot kT}{C_L} \quad (7)$$

$\underbrace{\hspace{10em}}_{i_{nd}^2 \div \Delta f} \quad \underbrace{\hspace{2em}}_{r_o^2} \quad \underbrace{\hspace{10em}}_{ENBW}$

$M_{Load}$  contributes noise to the output node in a similar fashion, but its associated noise current is less significant because of its smaller transconductance. Combining the noise due to  $M2$  and  $M_{Load}$  with the stage 1 noise and multiplying by 2 to account for each path of the differential circuit yields the following approximation for output referred noise of the entire circuit (for BJT operation).

$$v_{n\_tot}^2 = 2 \cdot \left[ \left( 1 + \frac{gm_{load}}{gm_2} \right) \cdot \frac{n \cdot kT}{2 \cdot C_L} + \frac{kT}{C_s} \right] \quad (8)$$

One expects that a transistor operating in subthreshold should yield noise somewhere between the MOS and BJT noise models, but we have found that Hspice simulations do not agree for small bias currents. Fig. 4 plots total integrated noise for different values of bias current in the source follower ( $C_L = 20pF$ ). Also plotted are the flat lines predicted by the equations above. As you can see, the simulation predicts that the noise approaches zero for biases of less than  $1 \mu A$ , even though transient simulations show that the transistor works properly (SFDR > 90dB) down to bias currents less than 200 nA. While a more thorough analysis is required to prove the Hspice model incorrect, our initial research implies that Hspice is not properly calculating transistor noise at extremely low bias currents. Reference [7] shows that the BJT model for  $i_d$  noise is accurate down to the sub-nA level. Furthermore, [9] shows that the small signal gain,  $gm$ , is linearly proportional to  $I_d$  ( $\sim I_c$ ) down to the nA level as well. Therefore, we are more confident in our hand calculations for noise than in the unmodified Hspice simulations.

To correct for this discrepancy, we simulate the noise in our circuit using a much higher bias current than is used in the transient simulations. Although this solution does not properly account for changes in junction capacitances, it still gives a much better estimate of noise power than Hspice does on its own. Also, the large sizes of our input and load capacitances compared to the junction capacitances minimize the error associated with the different bias conditions.

The noise simulation is carried out in two parts. First, we use the complete circuit to simulate the track mode noise at the gate of  $M2$  with the input switch closed. Next, we simulate the hold mode noise at the output node with an

ideal voltage source connected to the gate of the source follower. Since the gain of our amplifier is unity, summing these two noise powers yields the final output referred noise.

### B. Signal Swing Considerations

Closely coupled to noise considerations is the amplitude of the signal of interest. Signal amplitude is generally restricted due to nonlinear circuit behavior (e.g. distortion). Large signals can have a significant impact on the overall biasing conditions of a circuit, effectively creating a situation of signal-dependent biasing, which fundamentally leads to nonlinear behavior.

Because clock-boosting allows for nearly rail-to-rail swings to be driven onto Cs, the limit to signal swing comes from the source follower and load. Fig. 5 presents a simple picture for analysis. The gate of M2 can be driven low (technically even below ground) with no problems. However, high voltages are a concern because there must be headroom for  $V_{ds}$  of  $M_{Load}$  plus  $V_{gs}$  of M2.  $M_{Load}$  needs to provide a constant current to M2 and maintain large impedance, so  $V_{ds}$  of at least 400 mV is required for this device. M2 is operated in subthreshold, so its  $V_{gs}$  is less than 400 mV. Based on this analysis, a single ended peak-to-peak signal swing of 1 V is a good starting point for the design. Detailed investigation of the tradeoff between SNR and distortion for larger signal swings was left to the MATLAB pseudo-optimizer (see section F).

### C. Buffer linearity considerations

It is shown in [10] that the primary source of distortion in a source follower stems from the body effect. By using a PMOS source follower with its body tied to its source, we eliminate body effect in our design and thereby greatly increase our achievable SFDR. In addition, simulations show that distortion in the source follower is mainly quadratic and is further rejected by our differential topology. The remaining higher order distortion terms are difficult to characterize accurately by hand, so we relied on DC sweep data extracted from simulations to further optimize the source follower and PMOS load. By fitting a third order polynomial to simulation results, we were able to use equation (9) from [10] to generate Fig. 6, which shows how HD3 varies as a function of a number of parameters.

$$HD3 = \frac{c_3 V_i^2}{4c_1} \quad (9)$$

In this equation,  $V_i$  is the input amplitude,  $c_1$  is the coefficient of the first order term, and  $c_3$  is the coefficient of the third order term.

### D. Input switch considerations

The MOSFETs used to realize the sampling switches are often critical in low-distortion designs. Clock-boosting is most often employed in order to maintain linear ON-resistance of these switches across the full input range. This design utilizes clock boosting, but the decision to do so was only partially driven by concerns over the linearity of the switch resistance. Fig. 7 hints at the reason why. Suppose

the ON-resistance of the FET switch is modulated from 100 to 200 Ohms by the input signal. At high-frequencies, this can be a major problem because circuit input capacitance works with the ON-resistance to create a nonlinear voltage divider. But at the relatively low frequencies used in our design, the impedance of the input capacitance is still fairly large and the effect of this voltage divider is minimal. Therefore, nonlinear ON-resistance only causes moderate distortion.

Because an open loop design cannot accommodate bottom-plate sampling, the bigger problem with switches is signal-dependent charge injection. As a result, small switches are actually preferred. Fortunately, clock boosting allows even small switches to maintain excellent ON-resistance linearity, and directly helps to reduce input-signal modulation of charge injection [6].

### E. Settling considerations

In this design, settling analysis differs substantially from that of a closed loop design, but the high-level objective must not be lost: the circuit must be able to track and hold +/- FSR/2 signals alternating on every sample. In this case, settling happens during track mode. Fig. 8 shows the relevant timing diagram.  $V_{out}$  is initially held constant during HOLD mode while  $V_{in}$  changes to a new value. Once the circuit goes back into TRACK phase, it must remain in TRACK long enough for the output to settle to the new value of  $V_{in}$ .

Settling is clearly not symmetrical. For negative steps, M2 can rapidly discharge  $C_L$ , whereas for positive steps  $C_L$  must be charged by the bias source. This is demonstrated in Fig. 9, where M2 actually turns off and  $V_{out}$  slews by a rate equal to  $I_b/C_L$ . As a result, under worst case settling conditions the common mode output of the circuit will exhibit spikes which will need to be rejected by subsequent stages. The worst case settling error can be analyzed by examining a step at the input from  $-FSR/2$  to  $+FSR/2$ . For  $C_L = 16$  pF and a 100 kS/s rate,  $I_b$  must at least be greater than 3.2  $\mu$ A for the circuit to settle in time. Figs. 10 and 11 show plots of the simulated settling of our circuit for an input step from  $-1$  V to  $+1$  V.

### F. Circuit optimization

To improve upon our hand-calculated designs, we used a set of scripts capable of combining Hspice simulations and MATLAB analysis through a simple file-based communication scheme. First, MATLAB would generate Hspice parameter files in which each design variable was increased or decreased by a small amount from its hand-calculated value. A shell script would then use these parameter files in a series of Hspice simulations and pass the results back to MATLAB. By interpolating between the simulation results, MATLAB would choose a new, improved set of parameters and pass them back to the shell script. This loop could be repeated ad infinitum and required no human intervention. After several hours, the scripts settled on a "pseudo-optimal" design. Although the scripts were not guaranteed to find a global optimum, running them overnight often improved the FOM of our

circuit by a factor of 5 or 10 over the hand calculated design. Fig. 12 shows a typical plot of FOM vs. simulation number for an overnight run. Although they took nearly two weeks to develop, the scripts enabled us to compare optimized FOM's for several different designs quickly and easily. They also allowed us to tweak our final design in the background while writing this report.

### G. Theoretical Limits to FOM

Ultimate FOM limitations for this topology can also be derived by making a few assumptions. In a best case scenario, the circuit will be noise limited, even when accommodating an FSR of  $2 \cdot V_{dd}$ . Therefore, SNDR reduces to SNR given by:

$$\text{SNR} = \frac{\frac{(2V_{dd})^2}{2}}{2 \cdot \left( \frac{kT}{C_s} + \frac{kT}{C_L} \right)} = \frac{V_{dd}^2}{2 \cdot \frac{kT}{C}} \quad (10)$$

Note that this equation assumes that the output contributes noise proportional to  $kT/C$  and, therefore, that the optimal case occurs when  $C_s = C_L$ . Next, assume that the minimum bias current for the follower is that required to completely charge  $C_L$  to  $V_{dd}$  in one sample period and that this is all the power consumed by the circuit:

$$I_b = 2V_{dd} \cdot C_L \cdot f_s \quad P_{\text{ckt}} = 2 \cdot I_b \cdot V_{dd} \quad (11)$$

Under these conditions, the FOM simplifies to

$$\text{FOM} = \frac{f_s \cdot \text{SNR}}{P_{\text{ckt}} + P_{\text{drive}}} = \frac{1}{2 \cdot kT \cdot (3\pi + 2)} = 1.057 \times 10^{19} \frac{1}{\text{J}} \quad (12)$$

In other words, the maximum FOM for this architecture is around  $10^{19}$ .

### III SIMULATED PERFORMANCE

Figure 13 shows the testbench setup used for Hspice simulations. Table 1 compares the hand calculated starting parameters to their optimized final values, while Table 2 compares the estimated performance of our circuit to simulation results. Figures 14 and 15 show the noise spectral density and noise integrals during the TRACK and HOLD phases, respectively. Figure 16 plots a 32 point FFT of the output using an input sinusoid with  $f_{in} = \frac{15}{32} f_s$ .

Our circuit falls short of the theoretical maximum by about one order of magnitude. The primary reasons are that our signal swing is smaller than  $2 \cdot V_{dd}$ , the distortion power is comparable to the noise power, and there is a significant amount of power overhead that is not directly "useful" in charging signal capacitors (bias network, parasitics, etc). Ultimately, however, we are pleased with our circuit performance compared to the theoretical maximum.

**Table 1**

Parameter	Initial Value	Final Value
$C_s$	20 pF	23 pF
$C_L$	20 pF	16 pF
$W_1$	10 $\mu\text{m}$	5 $\mu\text{m}$
$L_1$	.18 $\mu\text{m}$	.18 $\mu\text{m}$
$W_2$	100 $\mu\text{m}$	250 $\mu\text{m}$
$L_2$	1.8 $\mu\text{m}$	.79 $\mu\text{m}$
$W_{\text{Load}}$	100 $\mu\text{m}$	36 $\mu\text{m}$
$L_{\text{Load}}$	1.8 $\mu\text{m}$	3.1 $\mu\text{m}$
$I_b$	3.2 $\mu\text{A}$	6 $\mu\text{A}$
$f_s$	100 kHz	100 kHz
$V_{ic}$	.4 V	.5 V
FSR	1.6 V	2 V

**Table 2**

Performance	Predicted	Simulated
Power Dissipation	24 $\mu\text{W}$	25 $\mu\text{W}$
Drive Power	39 $\mu\text{W}$	39 $\mu\text{W}$
Track Mode Noise	19 $\mu\text{V}_{\text{RMS}}$	21 $\mu\text{V}$
Hold Mode Noise	20 $\mu\text{V}_{\text{RMS}}$	22 $\mu\text{V}$
SFDR	90 dB	92.2 dB
SNDR	84.5 dB	86.1 dB
FOM	$4.5 \times 10^{17}$	$6.4 \times 10^{17}$

### IV. CONCLUSION

We have presented our design methodology for a PMOS source follower track and hold circuit. Our design uses clock boosting and subthreshold operation to achieve a SNDR of 86 dB at 100 kS/s with a 2 V FSR and power dissipation of 25  $\mu\text{W}$ . The final FOM is  $6.4 \times 10^{17}$ .

### V. REFERENCES

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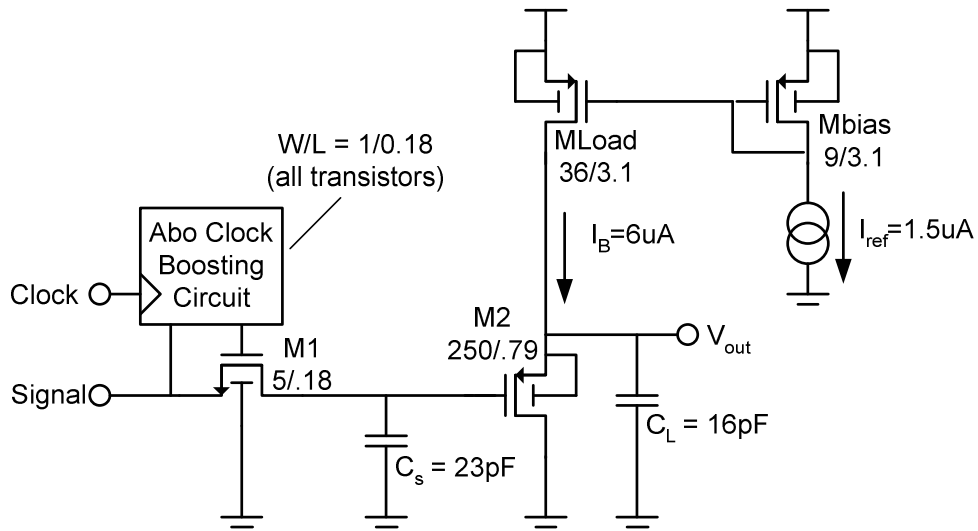


Fig. 1 Final design half circuit (bias transistor is shared by both half circuits)

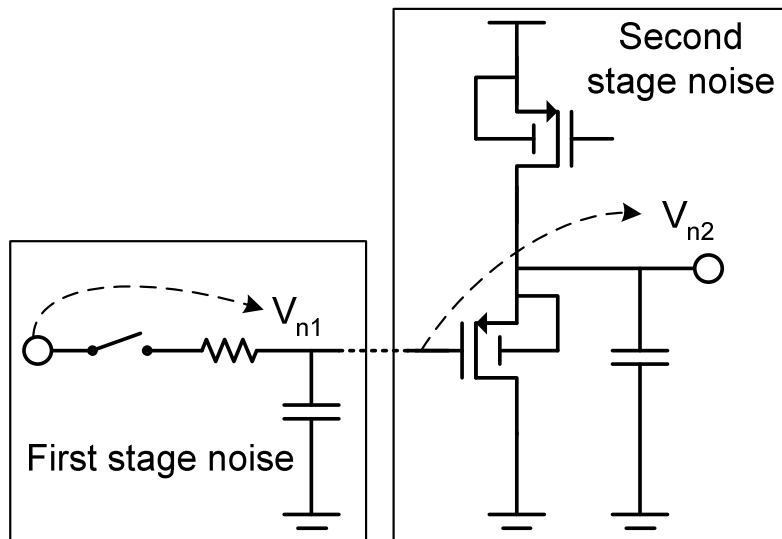


Fig. 2 Simplified circuit for noise analysis

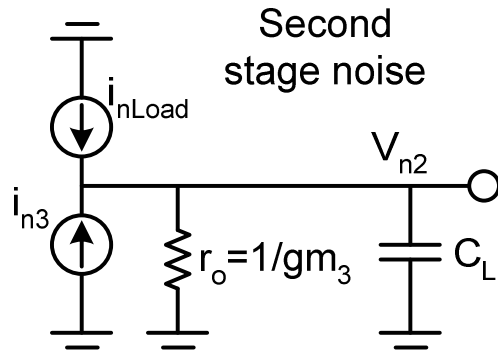


Fig. 3 Equivalent circuit for second stage noise analysis

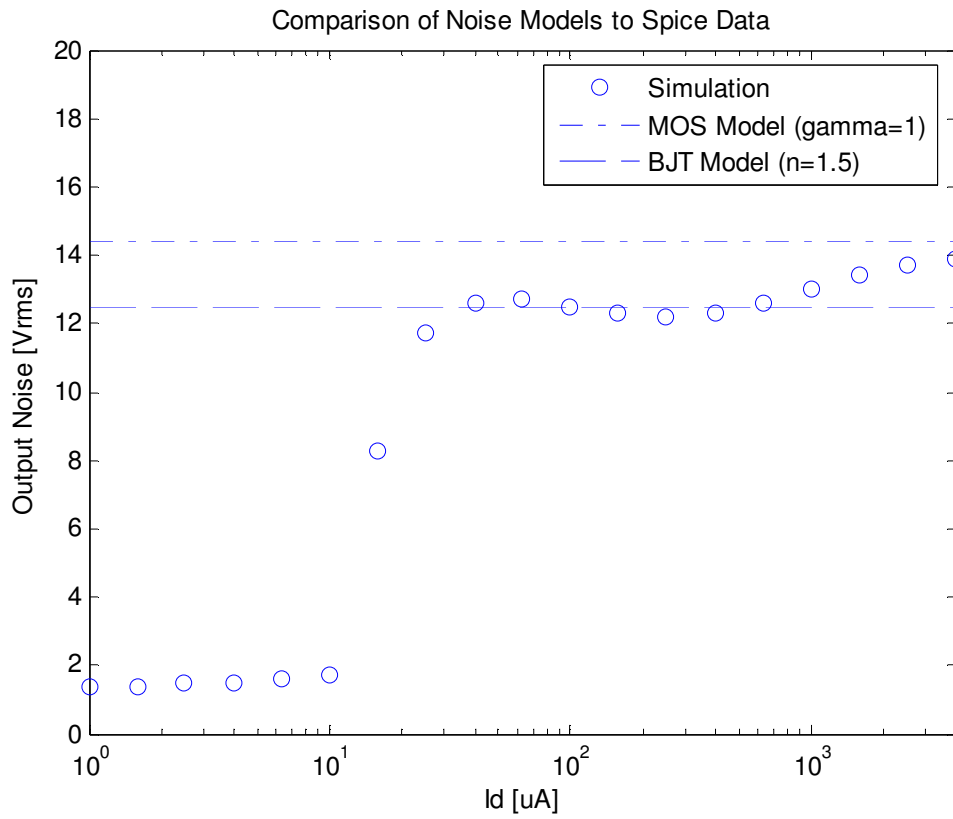


Fig. 4 Comparison of total integrated noise as calculated by Hspice vs. by hand

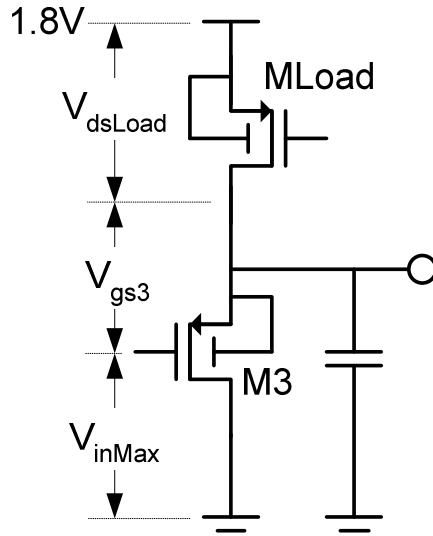


Fig. 5 Analysis of voltage swing limitations

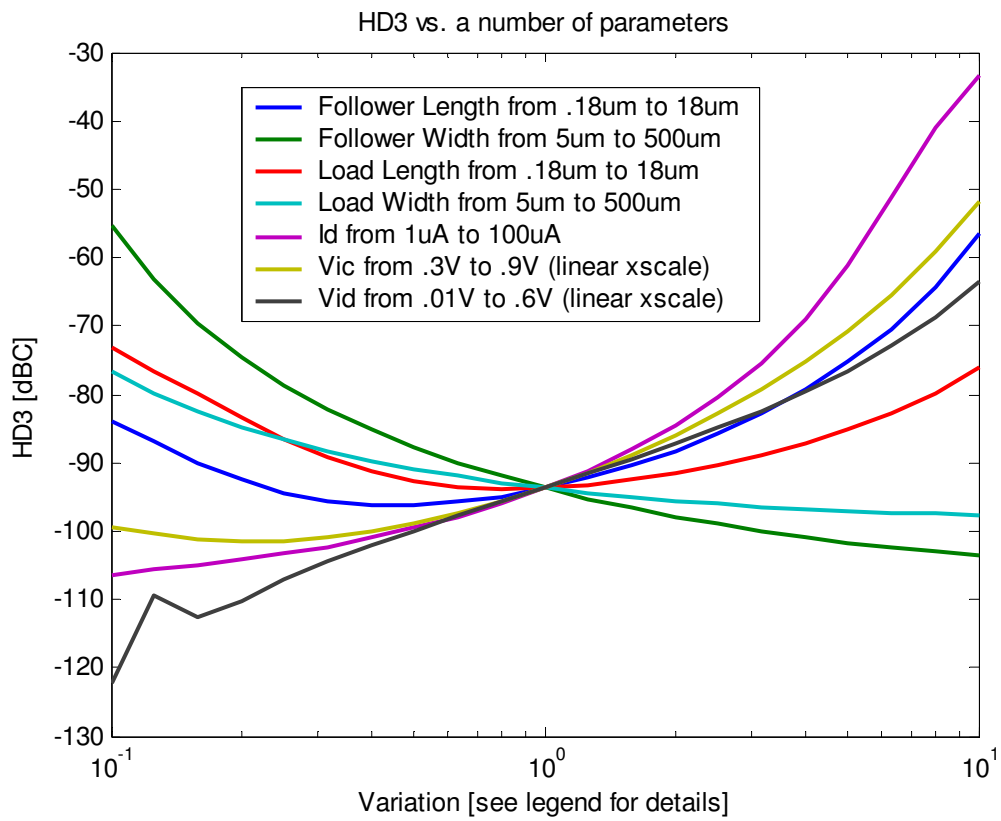


Fig. 6 Estimated HD3 based on DC sweeps of various parameters of the source-follower

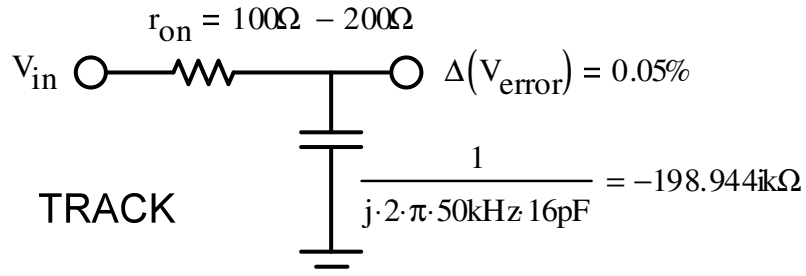


Fig. 7 Example of the effects of input switch resistance modulation

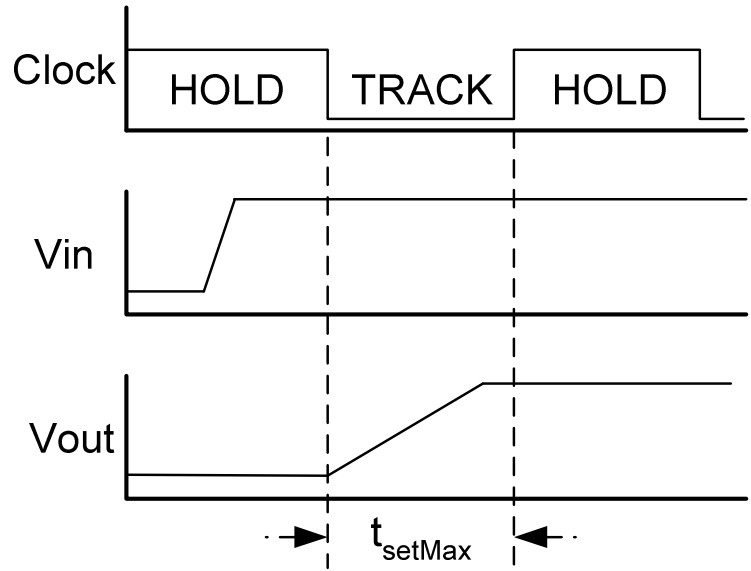


Fig. 8 Modified timing diagram for settling-time analysis

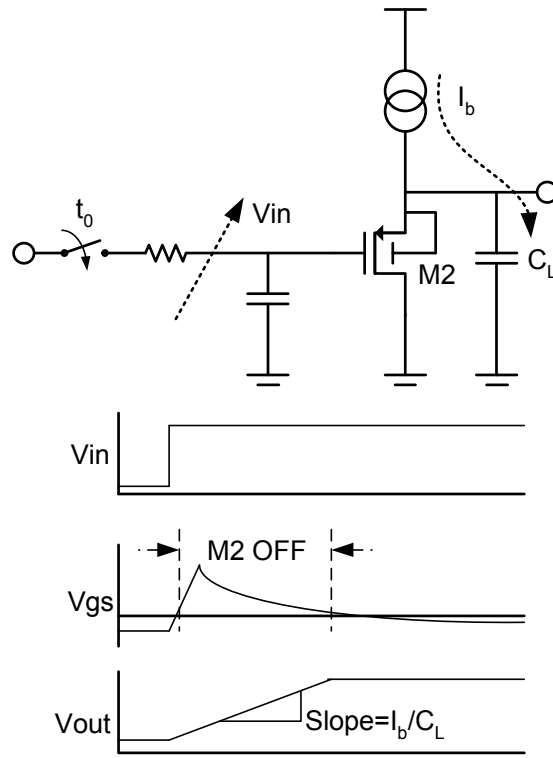


Fig. 9 Circuit and timing diagram for positive input step

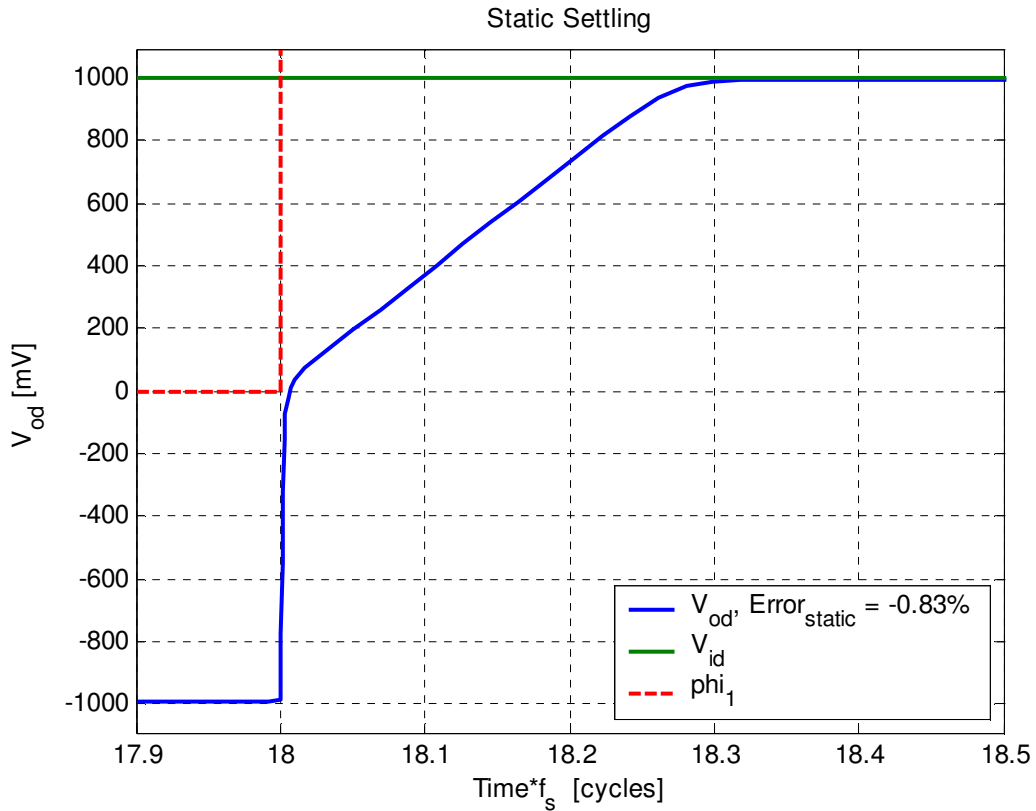


Fig. 10 Simulated settling results. The step part of the curve represents the quick discharge of  $C_L^-$  while the slow part of the curve results from the charging of  $C_L^+$  by  $I_B$ .

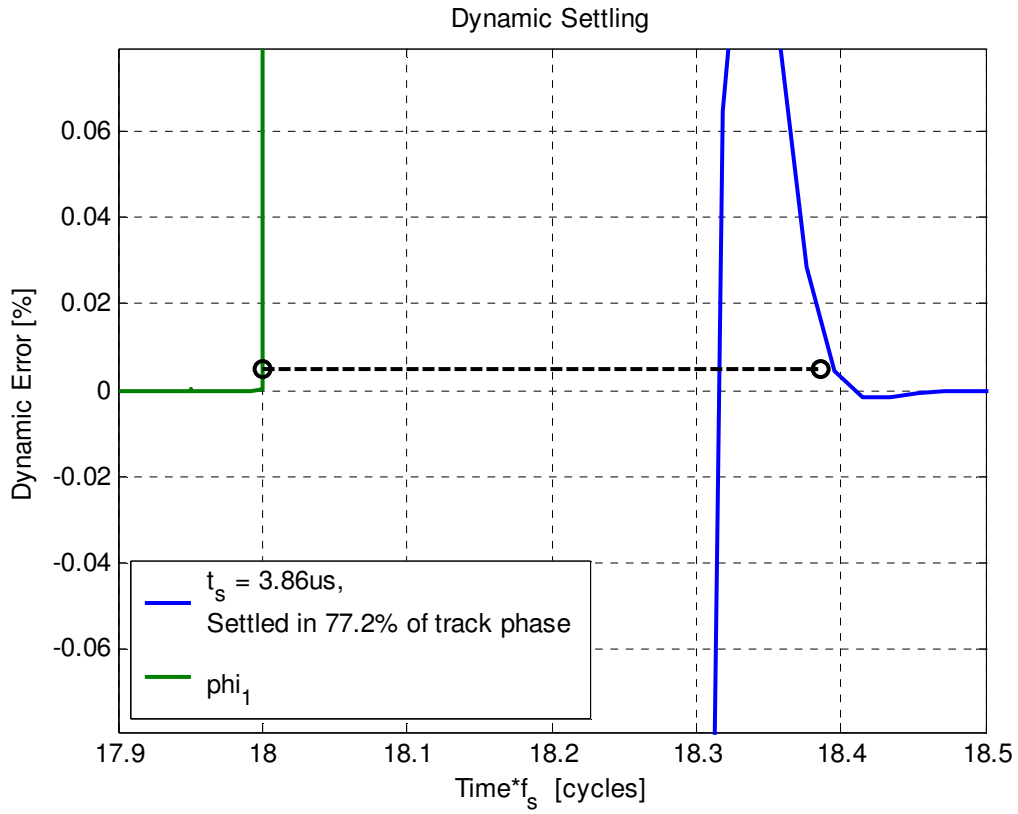


Fig. 11 Simulated settling results showing Dynamic Error

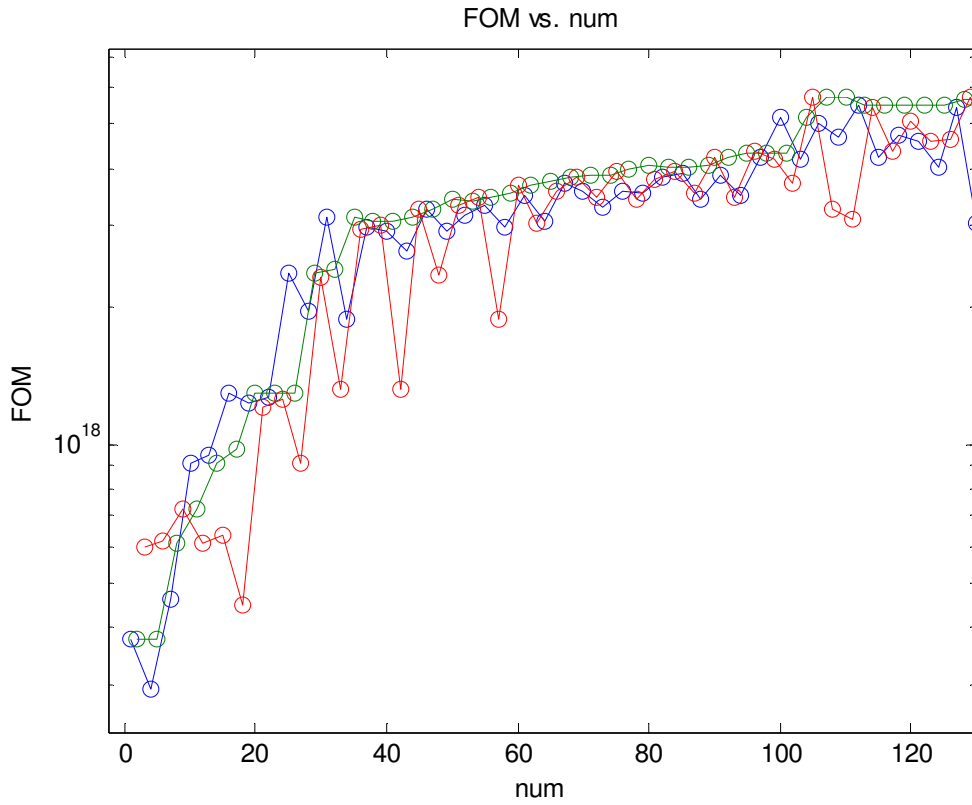


Fig. 12 MATLAB Optimization Results

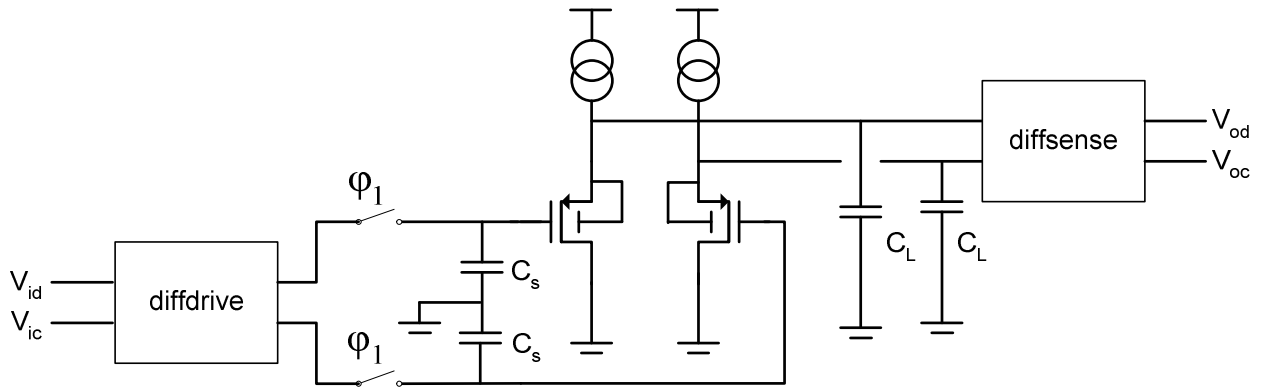


Fig. 13 Test bench setup

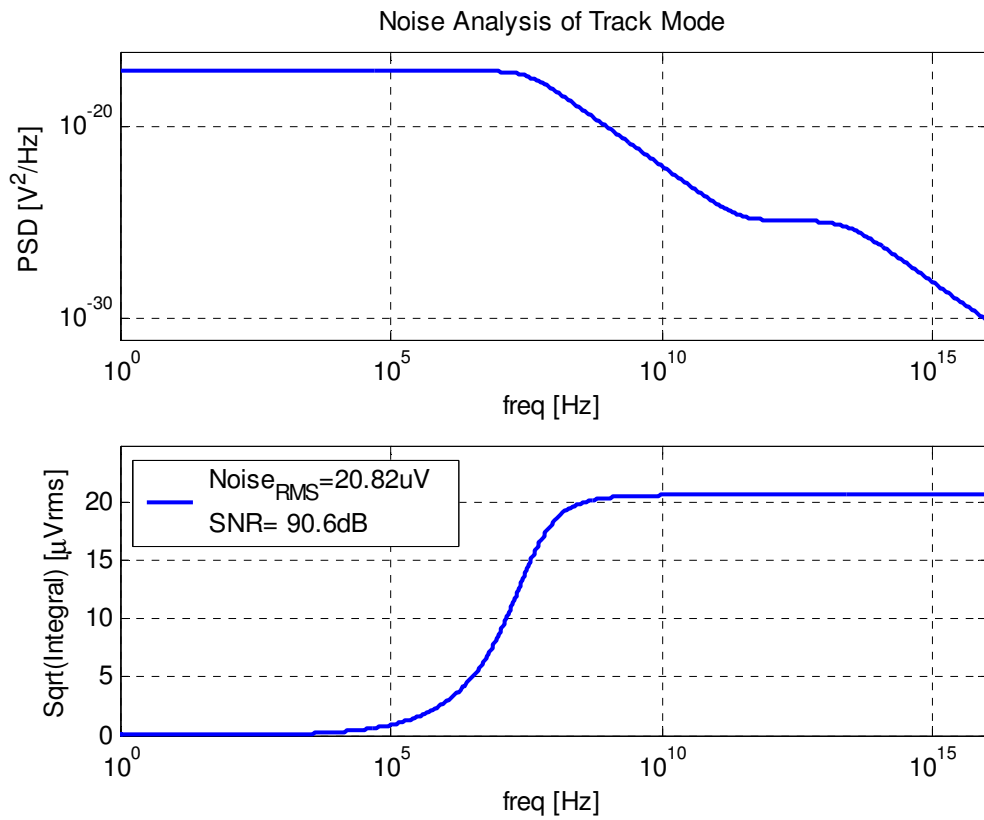


Fig. 14 Simulated noise during the track phase

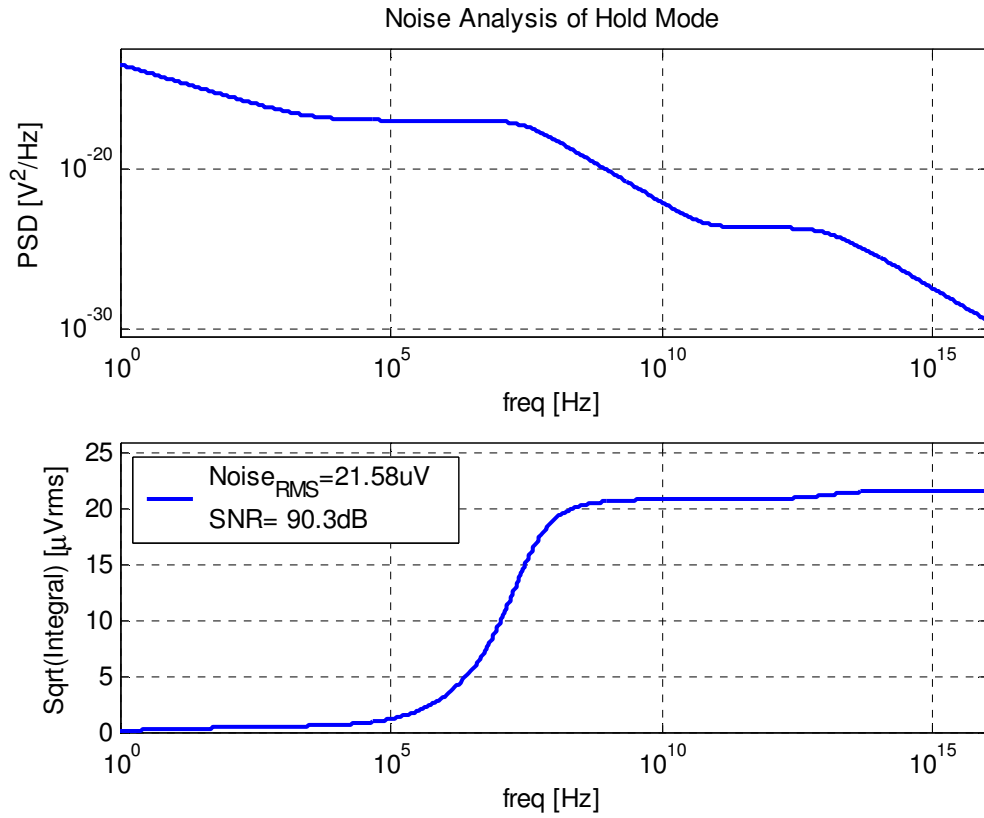


Fig. 15 Simulated noise during the hold phase

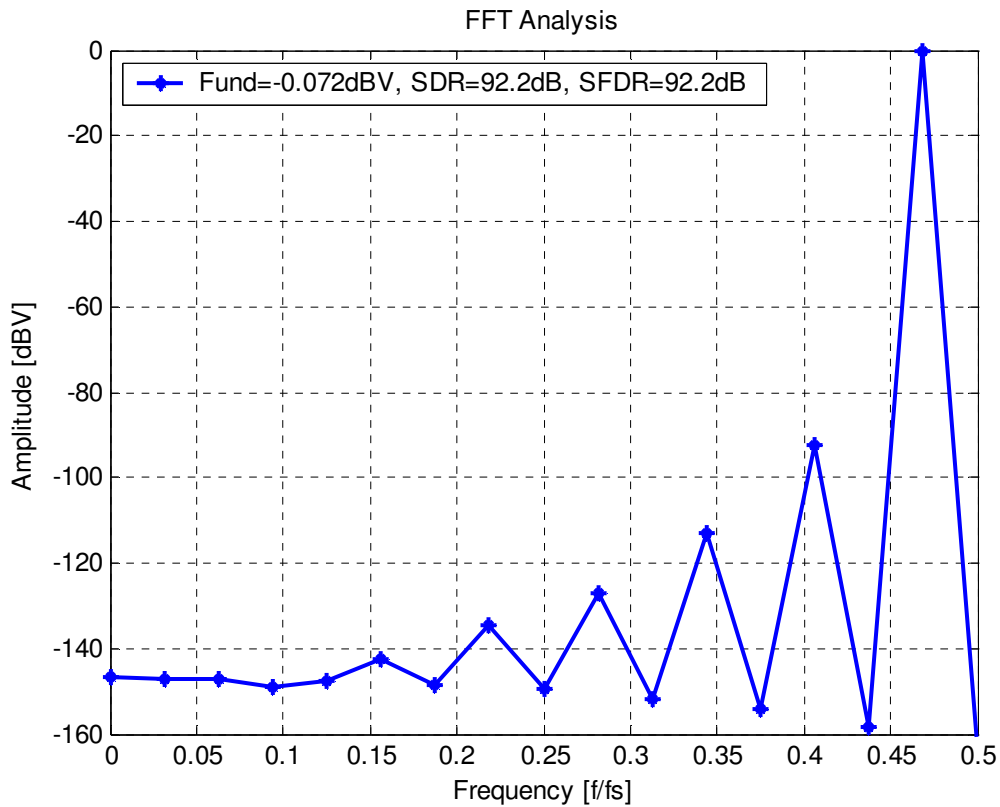


Fig. 16 A 32-point FFT with an input signal of  $f_s * 15/32$