

Benjamin C. Lee

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Interests

Scalable technologies :: emerging memory technologies, process variations, efficient circuits
Power-efficient architectures :: adaptive, heterogeneous, accelerated microprocessors
High-performance applications :: numerical methods, parallel computing, scientific computing
Statistical inference :: efficient modeling, optimization for computer systems
Technology policy :: technology, economics, policy for environmentally sustainable IT

Education

Harvard University Ph.D., Computer Science (2008).
Minor, Statistics.

Harvard University S.M., Computer Science (2006).

University of California, Berkeley B.S., Electrical Engineering and Computer Science (2004).
Minor, Business Administration.

Experience

Stanford University :: Electrical Engineering

Computing Innovation Fellow :: 9/09 – present

- Work with M. Horowitz to coordinate circuit, architecture, application design methods.
- Investigate accelerators, application-specific integrated circuits for energy efficiency.
- Optimize energy efficiency of varied instruction sets and novel applications.

Microsoft Research :: Computer Architecture Group

Post-doctoral Researcher :: 7/08 – 8/09

- Worked with D. Burger to study power-efficient technologies and systems.
- Investigated emerging scalable memory technologies (e.g., phase change memory).
- Analyzed performance, power efficiency of data center applications, hardware.

Harvard University :: School of Engineering and Applied Sciences

Graduate Researcher :: 9/04 – 6/08

- Worked with D. Brooks to model power-efficient, high-performance architectures.
- Performed robust spline-based regression for microprocessor performance, power.
- Enabled new capabilities in comprehensive optimization for emerging design priorities.

Intel Corporation :: Microarchitecture Research Laboratory

Intern Researcher :: 6/07 – 12/07

- Worked with H. Wang to construct scalable multiprocessor regression models.
- Constructed regression models for uniprocessor cores using product simulators.
- Constructed ancillary models to estimate multicore contention, system performance.

Lawrence Livermore National Laboratory :: Center for Applied Scientific Computing

Intern Researcher :: 6/06 – 9/06

- Worked with B. de Supinski to model parallel performance of numerical methods.
- Performed robust spline-based regression for multigrid, linear algebra performance.
- Compared accuracy, costs of regression, neural networks for Blue Gene/L performance.

University of California, Berkeley :: Computer Science Division

Undergraduate Researcher :: 1/02 – 8/04

- Worked with J. Demmel, K. Yelick to optimize scientific computing kernels.
- Optimized sparse symmetric matrix multiplication for 2.6x speedup, 0.5x storage.
- Derived analytical performance models based on system, application parameters.

Charles M. Salter Associates :: Airport Noise Modeling

Intern Engineer :: 6/00 – 8/00

- Worked with J. Freytag to prepare acoustical study for San Jose Airport.
- Collected, analyzed acoustical field data from airport residential areas in Excel/Access.

Honors

- 2009 National Science Foundation Computing Innovation Fellowship.
- 2008 Nominee, Best Paper, Int'l. Symp. Microarchitecture.
Nominee, ACM Doctoral Dissertation Award.
Invited Participant, St. Gallen Symposium.
- 2007 Invited Participant, St. Gallen Symposium.
- 2006 First Place, ACM Student Research Competition, Supercomputing.
- 2004 Harvard University Engineering and Applied Sciences Fellowship.
Best Paper, Int'l Conf. Parallel Processing.
- 2002 Finalist, Best Student Paper, Supercomputing.
- 2000 UC Berkeley National Merit Scholar.

Publications

Refereed Conferences and Journals

- [P1] Jeremy Condit, Edmund Nightingale, Christopher Frost, Engin Ipek, Benjamin Lee, Doug Burger, Derrick Coetzee. **"Better I/O through byte-addressable, persistent memory."** SOSP: Proc. 22nd Symposium on Operating Systems Principles. Big Sky, MT, October 2009.
- [P2] Kristen Lovin, Benjamin Lee, Xiaoyao Liang, David Brooks, Gu-Yeon Wei. **"Empirical performance models for 3T1D memories."** ICCD: Proc. 27th International Conference on Computer Design. Lake Tahoe, CA, October 2009.
- [P3] Xiaoyao Liang, Benjamin Lee, Gu-Yeon Wei, David Brooks. **"Design and test strategies for microarchitectural post-fabrication tuning."** ICCD: Proc. 27th International Conference on Computer Design. Lake Tahoe, CA, October 2009.
- [P4] Benjamin Lee, Engin Ipek, Onur Mutlu, Doug Burger. **"Architecting phase change memory as a scalable DRAM alternative."** ISCA: Proc. 36th International Symposium on Computer Architecture. Austin, TX, June 2009.
- nominee,
best paper* [P5] Benjamin Lee, Jamison Collins, Hong Wang, David Brooks. **"CPR: Composable performance regression for scalable multiprocessor models."** MICRO: Proc. 41st International Symposium on Microarchitecture. Como, Italy, November 2008.
- [P6] Benjamin Lee. **"Corporate social responsibility and the globalization of 'local values'."** 38th St. Gallen Symposium: Global Capitalism – Local Values. St. Gallen, Switzerland, May 2008.
- [P7] Benjamin Lee, David Brooks. **"Potential performance and power efficiencies from comprehensive microarchitectural adaptivity."** ASPLOS: Proc. 13th International Conference on Architectural Support for Programming Languages and Operating Systems. Seattle, WA, March 2008.
- [P8] Benjamin Lee, David Brooks. **"Roughness of microarchitectural design topologies and its implications for optimization."** HPCA: Proc. 14th International Symposium on High Performance Computer Architecture. Salt Lake City, UT, February 2008.
- [P9] Benjamin Lee. **"Flattening the world efficiently: Digital sustainability for the twenty-first century."** 37th St. Gallen Symposium: The Power of Natural Resources. St. Gallen, Switzerland, May 2007.
- [P10] Benjamin Lee, David Brooks. **"A tutorial in spatial sampling and regression strategies for microarchitectural analysis."** IEEE Micro Special Issue: Hot Tutorials, May/June 2007.
- [P11] Benjamin Lee, David Brooks, Bronis de Supinski, Martin Schulz, Karan Singh, Sally McKee. **"Methods of inference and learning for performance modeling of parallel applications."** PPOPP: Proc. 12th Symposium on Principles and Practice of Parallel Programming. San Jose, CA, March 2007.
- [P12] Benjamin Lee, David Brooks. **"Illustrative design space studies with microarchitectural regression models."** HPCA: Proc. 13th International Symposium on High-Performance Computer Architecture. Phoenix, AZ, February 2007.
- [P13] Benjamin Lee, David Brooks. **"Accurate and efficient regression modeling for microarchitectural performance and power prediction."** ASPLOS: Proc. 12th

International Conference on Architectural Support for Programming Languages and Operating Systems. San Jose, CA, October 2006.

[P14] Yingmin Li, Benjamin Lee, David Brooks, Zhigang Hu, Kevin Skadron. **“Impact of thermal constraints on multi-core architectures.”** IThERM: Proc. 10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems. Orlando, FL, May 2006.

[P15] Yingmin Li, Benjamin Lee, David Brooks, Zhigang Hu, Kevin Skadron. **“CMP design space exploration subject to physical constraints.”** HPCA: Proc. 12th International Symposium on High-Performance Computer Architecture. Austin, TX, February 2006.

*winner,
best paper*

[P16] Benjamin Lee, Richard Vuduc, James Demmel, Katherine Yelick. **“Performance models for evaluation and automatic tuning of symmetric sparse matrix-vector multiply.”** ICPP: Proc. 33rd International Conference on Parallel Processing. Montreal, Quebec, Canada, August 2004.

*finalist, best
student paper*

[P17] Richard Vuduc, James Demmel, Katherine Yelick, Shoaib Kamil, Rajesh Nishtala, Benjamin Lee. **“Performance optimizations and bounds for sparse matrix-vector multiply.”** SC02: Proc. Supercomputing. Baltimore, MD, November 2002.

Refereed Workshops

[P18] Benjamin Lee, David Brooks. **“Statistically rigorous regression modeling for the microprocessor design space.”** MoBS: Proc. Workshop on Modeling, Benchmarking, and Simulation in conjunction with ISCA-33. Boston, MA, June 2006.

[P19] Benjamin Lee, David Brooks. **“Effects of pipeline complexity on SMT/CMP power-performance efficiency.”** WCED: Proc. Workshop on Complexity Effective Design in conjunction with ISCA-32. Madison, WI, June 2005.

Technical Reports and Manuscripts

[P20] Vijay Janapa Reddi, Benjamin Lee, Trishul Chilimbi, Kushagra Vaid. **“Web search using small cores: Quantifying the price of efficiency.”** Technical Report MSR-TR-2009-105, Microsoft Research, August 2009.

[P21] Xiaoyao Liang, Benjamin Lee, Gu-Yeon Wei, David Brooks. **“Design and test strategies for microarchitectural post-fabrication tuning.”** Technical Report TR-06-08, Harvard University, December 2008.

[P22] Kristen Lovin, Benjamin Lee, Xiaoyao Liang, David Brooks, Gu-Yeon Wei. **“Empirical performance models for 3T1D memories.”** Technical Report TR-03-08, Harvard University, October 2008.

*nominee, ACM
dissertation
award*

[P23] Benjamin Lee. **“Statistical inference for efficient microarchitectural analysis.”** PhD Thesis, Harvard University, May 2008.

[P24] Benjamin Lee, Martin Schulz, Bronis de Supinski. **“Regression strategies for parameter space exploration: A case study in semicoarsening multigrid and R.”** Technical Report UCRL-TR-224851, Lawrence Livermore National Laboratory, September 2006.

[P25] Benjamin Lee, David Brooks. **“Regression modeling strategies for microarchitectural performance and power prediction.”** Technical Report TR-08-06, Harvard University, March 2006.

[P26] Benjamin Lee. **“An architectural assessment of SPEC CPU benchmark relevance.”** Technical Report TR-02-06, Harvard University, January 2006.

[P27] Benjamin Lee, Richard Vuduc, James Demmel, Katherine Yelick, Michael de Lorimier, Lijue Zhong. **“Performance optimizations and bounds for sparse symmetric matrix-multiple vector multiply.”** Technical Report UCB/CSD-03-1297, University of California, Berkeley, November 2003.

Talks

Conferences and Workshops

[T1] **“Architecting phase change memory as a scalable DRAM alternative.”** ISCA: International Symposium on Computer Architecture, June 2009.

- [T2] **“CPR: Composable performance regression for scalable multiprocessor models.”** MICRO: International Symposium on Microarchitecture, November 2008.
- [T3] **“Potential performance and power efficiencies from comprehensive microarchitectural adaptivity.”** ASPLOS: International Conference on Architectural Support for Programming Languages and Operating Systems, March 2008.
- [T4] **“Roughness of microarchitectural design topologies and its implications for optimization.”** HPCA: International Symposium on High Performance Computer Architecture, February 2008.
- [T5] **“Methods of inference and learning for performance modeling of parallel applications.”** PPOPP: Symposium on Principles and Practice of Parallel Programming, March 2007.
- [T6] **“Statistical inference for efficient microarchitectural analysis.”** BARC: Boston Area Architecture Workshop, January 2007.
- [T7] **“Illustrative design space studies with microarchitectural regression models.”** HPCA: International Symposium on High Performance Computer Architecture, February 2007.
- [T8] **“Statistical inference for efficient microarchitectural and application analysis.”** SC06: Supercomputing, November 2006.
- [T9] **“Accurate and efficient regression modeling for microarchitectural performance and power prediction.”** ASPLOS: International Conference on Architectural Support for Programming Languages and Operating Systems, October 2006.
- [T10] **“Statistically rigorous regression modeling for the microprocessor design space.”** MoBS: Workshop on Modeling, Benchmarking, and Simulation in conjunction with ISCA, June 2006.
- [T11] **“Effects of pipeline complexity on SMT/CMP power-performance efficiency.”** WCED: Workshop on Complexity Effective Design in conjunction with ISCA, June 2005.
- [T12] **“Performance models for evaluation and automatic tuning of symmetric sparse matrix-vector multiply.”** ICPP: International Conference on Parallel Processing, August 2004.
- [T13] **“Optimizations and bounds for sparse symmetric matrix-vector multiply.”** SIAM Conference on Parallel Processing for Scientific Computing, March 2004.

Technical Panels

- [T14] **“Emerging technologies.”** NANOARCH: International Symposium on Nanoscale Architectures in conjunction with DAC, July 2009.
- [T15] **“New memory technology.”** ISCA: International Symposium on Computer Architecture, June 2009.

Invited and Other

- [T16] **“Statistical inference for tractable architectural analysis.”** University of Texas at Austin, Swiss Federal Institute of Technology (ETH) Zurich, University of Rochester, Rutgers University, Northwestern University, February – April 2009.
- [T17] **“Statistical inference for efficient microarchitectural analysis.”** Microsoft Research Redmond, IBM Research Yorktown Heights, April 2008.
- [T18] **“CPR: Composable performance regression for scalable multiprocessor models.”** Intel Santa Clara, December 2007.
- [T19] **“Statistical inference for efficient microarchitectural analysis.”** Intel Santa Clara, Intel Folsom, June 2007.
- [T20] **“Regression modeling strategies for parameter space exploration.”** Lawrence Livermore National Laboratory, September 2006.
- [T21] **“Poster: Efficient design space exploration for chip multiprocessors.”** Harvard University Industrial Partnership Annual Meeting, October 2005.
- [T22] **“Poster: Automatic performance tuning of sparse matrix kernels.”** SIAM Conference

on Computational Science and Engineering, February 2003.

Artifacts

- [A1] CORE: Comprehensive Optimization via Regression Estimates (CORE) is a collection of example R scripts that construct microarchitectural performance, power regression models with correlation, association, clustering, significance analyses.
<http://www.eecs.harvard.edu/~bclee/software.html>
- [A2] OSKI: The Optimized Sparse Kernel Interface is a collection of low-level C primitives that provide automatically tuned computational kernels on sparse matrices for use in solver libraries and applications.
<http://bebop.cs.berkeley.edu/oski/>

Patents

- [IP1] Jeremy Condit, Edmund B. Nightingale, Benjamin Lee, Engin Ipek, Christopher Frost, Doug Burger. **"Hardware Support for Persistent Memory on a Memory Bus."** United States Patent. Application filed July 2009.
- [IP2] Jeremy Condit, Edmund B. Nightingale, Benjamin Lee, Engin Ipek, Christopher Frost, Doug Burger. **"Operating System Support for Persistent Memory on a Memory Bus."** United States Patent. Application filed June 2009.

Teaching

Harvard University :: School of Engineering and Applied Sciences

Teaching Fellow :: 9/05 – 6/08

- Spring 2008 :: Guest lecture on power modeling, digital sustainability (CS246).
- Fall 2006 :: Management of innovation in science, engineering (ES139/239).
- Spring 2006 :: Advanced architecture, power-aware systems (CS246).
- Fall 2005 :: Introductory computer architecture (CS146), digital logic design (CS141).

ASPLOS :: Architectural Support for Programming Languages and Operating Systems

Tutorial Co-Organizer :: 3/08

- Methods of Learning and Inference for Large Design and Parameter Spaces.
- With D. Brooks, B. de Supinski, S. McKee, M. Schulz, K. Singh.

ISCA :: International Symposium on Computer Architecture

Tutorial Co-Organizer :: 6/07

- Inference and Learning for Large Scale Microarchitectural Analysis.
- With D. Brooks, B. de Supinski, S. McKee, M. Schulz, K. Singh.

Service

Memberships

Member, Institute of Electrical and Electronics Engineers (IEEE)
Member, Association for Computing Machinery (ACM, SIGARCH)
Member, Society for Industrial and Applied Mathematics (SIAM)

Conference Service

Program Committee, Intl. Symposium Perf. Analysis of Systems & Software (ISPASS) 2010.
Co-Organizer, Workshop Emerging Memory Technologies (EMT) at ISCA 2009.
Program Committee, Workshop Modeling, Benchmarking, Simulation (MoBS) at ISCA 2009.
Publication Chair, Intl. Conf. Parallel Architectures & Compilation Techniques (PACT) 2009.
Program Committee, Intl. Symposium Perf. Analysis of Systems & Software (ISPASS) 2009.

Reviews

Architectural Support for Programming Languages and Operating Systems (ASPLOS)
Intl. Symp. High Performance Computer Architecture (HPCA)
Intl. Symp. Computer Architecture (ISCA)
Intl. Symp. Low Power Electronics and Design (ISLPED)
Intl. Symp. Perf. Analysis of Systems & Software (ISPASS)
Intl. Symp. on Microarchitecture (MICRO)
IEEE Transactions on Computers (TC)
IEEE Transactions on Parallel and Distributed Systems (TPDS)
IEEE Transactions on Very Large Scale Integration Systems (TVLSI)