A Four-Channel Beamforming Down-Converter in 90-nm CMOS Utilizing Phase-Oversampling

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***Abstract*—In this paper, a 4-GHz, four-channel, analog-beamforming direct-conversion down-converter in 90-nm CMOS is presented. Down-converting vector modulators (VMs) in each channel multiply the inputs with complex beamforming weights before summation between the different channels. The VMs are based on a phase-oversampling technique that allows the synthesis of inherently linear, high-resolution complex gains without complex variable gain amplifiers. A bank of simple passive mixers driven by a multiphase local oscillator (LO) in each VM performs accurate phase shifting with minimal signal distortion, and a pair of transimpedance amplifiers (TIAs) combines the mixer outputs to perform beamforming weighting and combining. Each individual channel achieves 360° phase shift and gain-setting programmability with 8-bit digital control, a complex gain constellation with a mean error-vector magnitude (EVM) of $<2\%$, and a measured phase error of $<$ 5.5° at a back-off of 4 dB from the maximum gain setting. The beamformer demonstrates $>$24-dB blocker rejection for blockers impinging from different directions and 17-dB signal EVM improvement in the presence of an in-channel blocker.**

***Index Terms*—Beamforming, Cartesian combining, dynamic range, mixer, multiphase local oscillator (LO), phased arrays, phase-oversampling, phase shifter, RF CMOS, receivers, RF variable gain amplifier (RFVGA), vector modulator (VM).**

I. Introduction

Among the many multi-antenna applications enabled by beamforming systems are interference cancellation for spectral reuse or dynamic range (DR) enhancement, beamsteering for spatially selective power gain, and spatial diversity. Beamforming can be performed completely in the digital domain to maximize flexibility, but this approach imposes stringent DR requirements on all analog blocks. Similarly, nonlinearity in amplifiers prior to the beamforming circuitry can also limit overall receiver DR. By performing high-resolution, analog-domain beamforming and signal combining early in the receive path and minimizing the number of nonlinear amplifying components, the DR of successive analog blocks can be relaxed and/or the receiver DR can be maximized.

High-resolution beamforming in the analog domain can be performed with vector modulators (VMs) and has been explored in Cartesian-combining architectures using high-resolution RF variable gain amplifiers (RFVGAs) [1]–[5] or bi-phase modulators [6], [7]. Tunable phase shifters used in phased array systems can also be augmented with RFVGAs to implement complex gain (phase shift and variable gain) operations [8]–[11]. All of these approaches are capable of synthesizing complex gains, but require complicated amplifiers or amplitude modulators in the signal path that may be nonlinear. Furthermore, due in part to lower supply voltages and degrading analog transistor metrics, a trend has emerged in deeply scaled CMOS nodes in which analog blocks are becoming simpler and analog circuit complexity is gradually being transferred to the supporting digital circuits or to the architectural level. Our proposed phase-oversampling and coarse quantization is one technique that retains the high-complex gain resolution of the previous approaches, yet also allows the circuit complexity of RFVGAs to be shifted to the architectural level, thus linearizing the receive paths [12].

In this paper, a 4-GHz direct-conversion CMOS beamforming IC fabricated in 90-nm CMOS based on phase-oversampling and coarse quantization is demonstrated. The chip contains four down-conversion channels, and the VM architecture implements beamforming functionality via multiphase local oscillator (LO) signals and current-domain mixer banks. Utilizing only simple core components and no RFVGAs, the chip achieves accurate complex gain control, beamsteering, and precise blocker cancellation in measurements. Thus, it demonstrates the inherent accuracy of the phase-oversampling architecture.

This paper is organized as follows. A theoretical overview of phase-oversampling VMs and the accompanying circuit architecture is given in Sections II and III, respectively. In Section IV, circuit-level implementation details of the multiphase LO generation and phase-oversampling, down-conversion VM blocks are discussed, followed by the presentation of measurement results in Section V and the conclusion in Section VI.

II. Analog-Domain Complex Gain

A. Cartesian-Combining VM

One way to realize a complex gain in the analog domain is with a VM utilizing RFVGAs with Cartesian combining [1]–[4]. One such structure is shown in Fig. 1(a). In this approach, the RF signal $(V_{\rm in})$ is split into a 0° phase-shift path and a 90° phase-shift path. Each phase is scaled by an RFVGA, and the

Manuscript received February 04, 2010; revised May 05, 2010; accepted June 24, 2010. Date of current version October 22, 2010. This paper was approved by Guest Editor Mototsugu Hamada. This work was supported in part by C2S2, a MARCO FCRP.

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Digital Object Identifier 10.1109/JSSC.2010.2063971

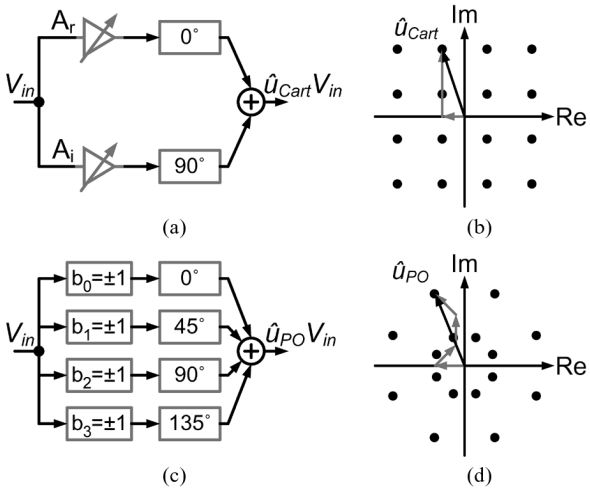

Fig. 1. VMs. (a) Cartesian-combining VM and (b) its complex gain constellation. (c) Phase-oversampling VM and (d) its complex gain constellation.

two are added together to synthesize a complex beamforming weight

$$\hat{u}_{Cart} = A_I e^{j0} + A_Q e^{j\frac{\pi}{2}}. \tag{1}$$

Fig. 1(b) and (1) demonstrate the synthesis of complex gain in a Cartesian-combining VM. If each RFVGA has a 2-bit resolution, consider the case in which the amplitude of the 0° phase is scaled by $-1/3$, and the amplitude of the 90° phase is scaled by $+1$. Superposition at the output of the two paths achieves the highlighted complex gain point in Fig. 1(b). A collection of all possible combinations of RFVGA settings results in the QAM-like, 16-point complex-gain constellation.[1]

In the Cartesian-combining VM, the phase domain is coarsely quantized—there are only two phases. Accurate complex gain is achieved through high gain resolution in the RFVGAs.

B. Phase-Oversampling VM

In a phase-oversampling VM, shown in Fig. 1(c), the phase domain is finely quantized, and the amplitude domain is coarsely quantized [12]. For a constant complex-gain resolution, as the number of phases is increased, the required amount of amplitude resolution for each RFVGA decreases. In the extreme case, the RFVGAs can be replaced with simple cross-coupled switches. Here, the RF signal is split into multiple phase-shift paths, and each path is scaled by a $+1$ or -1 coefficient. The complex gain of a phase-oversampling VM is given by

$$\hat{u}_{PO} = \frac{2}{M}\sum_{m=0}^{M-1} b_m e^{j\frac{m\pi}{M}} \tag{2}$$

where the exponential terms denote the phase shifts, each b_m term denotes the scaling coefficient for the m^{th} phase shifter, and M is the total number of phase shifters.

[1]Note that the constellation shown in Fig. 1(b) is not a demodulated signal constellation. Rather, it is a collection of the possible complex weights that can multiply the input signal in each channel.

Fig. 1(d) demonstrates the synthesis of a complex-gain point. Consider the case in which the 0°, 45°, 90°, and 135° phases are scaled by -1, $+1$, $+1$, and $+1$, respectively. The outputs of the phase shifters are added via superposition to generate a complex-gain point ($\hat{u}_{PO}$), highlighted in Fig. 1(d), which is close to the one highlighted in Fig. 1(b). A collection of all possible weight combinations results in the complex gain constellation in Fig. 1(d). Theoretically, with enough phases, every point that can be represented with a Cartesian-combining VM can also be represented with a phase-oversampling VM.

One advantage of using a phase-oversampling approach is that active nonlinear components can be removed from a receive channel. The RFVGAs in Cartesian-combining VMs can cause large close-in blockers to desensitize the receiver or corrupt a signal with blocker intermodulation products. In phase-oversampling VMs, the nonlinear amplifiers are replaced with cross-coupled switches, thus potentially linearizing the receive channel.

C. Accuracy and System Complexity Tradeoffs

The required resolution of a complex gain operation for beamforming varies from application to application. For example, in the demanding task of interference cancellation, the complex-gain resolution should be proportional to the desired cancellation accuracy, but this degree of resolution is not needed when the receive paths are utilized mainly for power gain or diversity.

Phase-oversampling VMs present a tradeoff between system complexity and the achievable complex-gain accuracy [12]. As the number of phase shifters M increases, complex-gain accuracy improves, but circuit complexity and its associated area and power consumption also increase. A value of $M = 8$ was chosen in this work as a compromise between these two factors.

The different phase shifts for phase-oversampling VMs are not orthogonal, so the mapping from complex-gain points to b_m switch coefficients is not straightforward. There are two basic approaches to perform this mapping: An exhaustive search of the mapping between b_m switch coefficients and complex-gain points can be performed. Alternatively, a $\Sigma\Delta$ algorithm running in the digital domain can be used to derive the coefficients b_m.

D. Component Choice of Phase Shifters

Both Cartesian-combining and phase-oversampling VMs synthesize tunable complex gains from nontunable phase shifters. Structures such as RC-CR networks are lossy, complicating their use in the signal path [8], [13]. Low-loss passive phase shifters can be realized with transmission lines or *LC* networks, but typically occupy a large area [14] and can introduce frequency-dependent phase shift and insertion loss if not precisely calibrated.

For these reasons, the phase shifters for the phase-oversampling VM prototype are implemented with mixers and multiphase LO signals. The exploitation of multiphase LO to establish the complex gain decouples the complexity of the phase-shift circuit from the signal integrity of the down-conversion channel. As long as the LO phases are accurate and the mixers switch completely, insertion loss and nonlinearity in the LO distribution path do not affect the quality of the received signal.

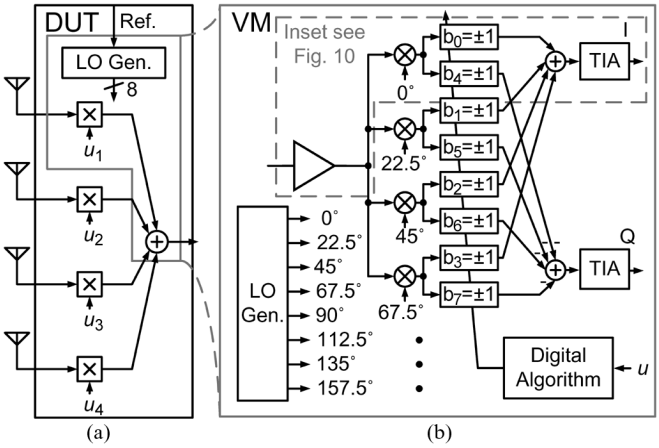

Fig. 2. Block diagram of the implemented phase-oversampling down-converter. (a) Full chip. (b) Single channel.

Phase shifting via the LO also allows the use of passive mixers, which avoids any nonlinear amplification in the down-conversion channel, further enhancing the receiver linearity.

III. System Architecture

A diagram of the implemented 4-GHz direct-conversion, phase-oversampling VM architecture is shown in Fig. 2(a) [15]. Here, the complex beamforming weights $u_1 - u_4$ can be chosen to steer the receiver in the direction of a received signal [16] and/or to actively cancel a blocker [17]. Four down-conversion channels are implemented on the test chip. Each channel is optimized for wideband OFDM signals such as 802.11a/g. The subcarrier at dc for such signals is typically discarded in these standards, so the direct-conversion architecture was chosen for its low component count and simplicity.

A. VM Implementation

A single down-conversion channel is shown in Fig. 2(b). Each VM consists of a transconductance (G_m) amplifier, a bank of eight mixers, a bank of cross-coupled nMOS switches, and a set of in-phase (I) and quadrature (Q) transimpedance amplifiers (TIAs). Each mixer is driven by a separate LO phase and phase-shifts the incoming signal during frequency translation. All signal lines in the channel are fully differential. A complex gain is realized by choosing the correct sign b_m for the output of each mixer and then summing across all mixers with the TIAs. The outputs of the 90°, 112.5°, 135°, and 157.5° mixers, which are not shown for simplicity, are multiplied by b_4, b_5, b_6, and b_7, respectively, before connecting to the I-TIA. The same mixer outputs are also multiplied by b_0, b_1, b_2, and b_3, respectively, for the Q-TIA. This cross-connecting approach allows the number of mixers to be halved, as is explained below.

B. Component Sharing

Because of the large number of components in each down-conversion channel, component sharing between different redundant circuit blocks was emphasized during the design process. Mixers are shared between the I- and Q-output for each VM down-conversion channel, the G_m stage is shared among the mixers in each channel, and the LO generation circuitry and TIAs are shared among all channels.

To demonstrate mixer sharing in a phase-oversampling VM, first consider a generalized VM with I- and Q-output as shown in Fig. 3(a). The RF signal is phase-shifted and scaled in gain before being split into two paths and phase-shifted by 0° and 90° to generate the I- and Q-output, respectively. If a phase-oversampling architecture with $M = 4$ is adopted, the VM is realized as shown in Fig. 3(b). Half of the phase shifters are redundant and can be merged. In Fig. 3(c), the outputs of the phase shifters are shared between the I- and Q-channel, thereby saving on area and LO distribution power. The extra -1 needed for the 0° and 45° phase shifters on the Q-channel shown in Fig. 3(c) are easily derived through cross-connecting the differential signals.

C. Multiphase LO Architectural Concerns

The LO generation block must ideally generate eight evenly spaced LO phases between 0° and 180° with low phase noise around 4 GHz. Ring oscillators can achieve both frequency and multiphase LO generation simultaneously, but typically suffer from higher phase noise than *LC*-type voltage-controlled oscillators (VCOs) [18]. Instead, a standard frequency synthesizer utilizing an *LC* VCO can generate a high-quality reference signal, and a separate block can be used to derive the multiphase LO signals. In this study, we have adopted the latter approach.

Passive structures such as polyphase filters [13] and interpolation networks [19] can be used to derive multiple LO phases or filter out phase errors in multiphase signals, but they typically introduce large insertion loss if the phase separation between adjacent inputs is large. Alternatively, if a purely active approach is taken to avoid insertion loss and the multiphase LO is generated directly via a delay-locked loop (DLL), a prohibitively low cell delay of approximately 15.6 ps is required. In the fabricated prototype, a DLL is used for coarse phase generation, and a passive interpolation network is used for fine phase generation along with a bank of edge combiners to achieve the best of both approaches. Because power consumption, complexity, and area tradeoff against LO phase accuracy, the LO generation block was centralized and shared between the different channels on the chip. Circuit-level implementation details of the LO generation blocks and VM channels are further discussed below.

IV. Circuit Design

A. Multiphase LO Generation

A block diagram of the multiphase LO generation circuit is shown in Fig. 4. A pseudo-differential DLL splits a reference signal running at $f_{\mathrm{LO}}/2$ into eight equally spaced phases. The eight DLL outputs are buffered and sent into a resistive interpolation network, which averages out the phase errors from the DLL and interpolates between them to produce 16 phases. The interpolator outputs are then edge-combined to produce eight phases at f_{LO} before being distributed to the mixer bank. All signals swing rail-to-rail to minimize the effect of mismatches. While generating the multiphase LO, each block adds mostly white noise, thus avoiding degradation of the LO's close-in phase noise performance. Though the averaging effect of the phase interpolator removes phase error to the first order, active

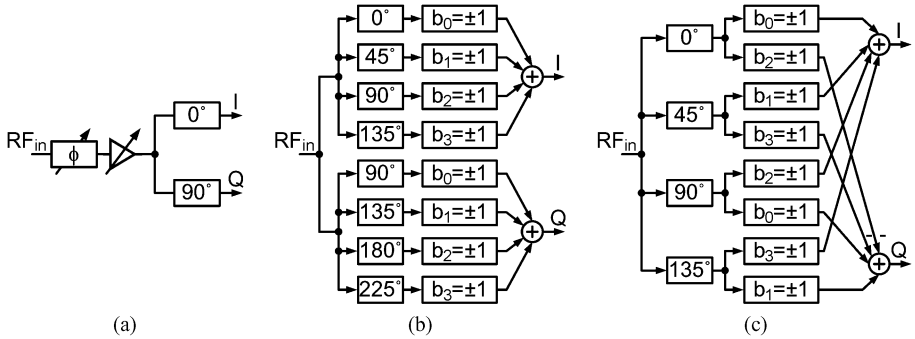

Fig. 3. IQ representation and mixer sharing. (a) VM with IQ outputs. (b) Phase-oversampling VM with IQ outputs. (c) VM with IQ outputs and merged phase shifters.

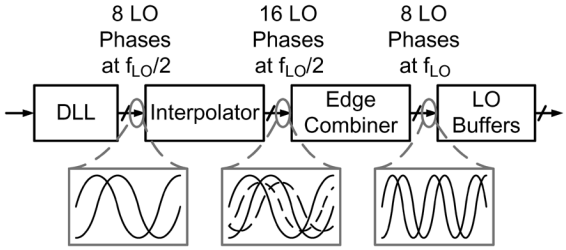

Fig. 4. LO generation block diagram.

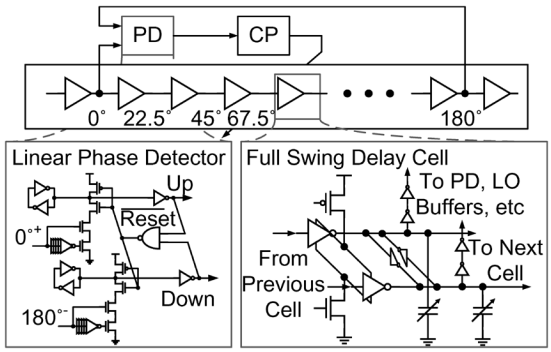

Fig. 5. DLL block diagram.

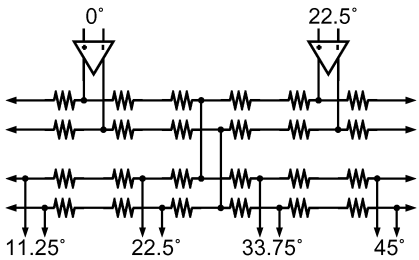

Fig. 6. Two-level resistive interpolation block.

device and layout mismatch can still introduce second-order phase mismatch. These can be calibrated by switched capacitor or tunable varactor loads at the LO buffer stages to compensate for residual phase error. Alternatively, if M is sufficiently large, the coefficients b_m can be "predistorted" to choose a different nearby complex gain point, and compensate for the LO phase mismatches.

Reducing the operating frequency increases the required DLL stage delay to approximately 31 ps. The DLL generates multiphase signals that are close enough to enable efficient interpolation between them, thereby greatly improving phase accuracy and reducing insertion loss in the passive network. If finer LO phase separation is required from the DLL, it could be designed to run in harmonic lock, with its multiphase outputs reordered appropriately.

1) DLL: A block diagram of the DLL used for coarse multiphase LO generation is shown in Fig. 5. The DLL is pseudo-differential and operates at $f_{\rm LO}/2$. The first delay cell and last two delay cells in the chain are dummy cells, inserted to equalize cell loading. The DLL locks to 180° instead of 360° by cross connecting the differential outputs of the last delay cell in the chain. This design choice reduces the number of delay cells by half, reducing power consumption and area, and conveniently avoids the stuck-lock condition [20]. A false-lock detector (not shown) and reset signal prevent the DLL from falling into harmonic lock [21].

Each delay cell consists of a current-starved inverter pair, which provides wide delay-tuning range and constant rail-to-rail output swing. This is in contrast to differential pair-based delay cells, where output swing can be a function of delay [22]. The current-starving transistors are shared between the positive and negative paths, so under starved conditions the delay cell still behaves differentially during input and output transitions. Each cell also contains a pair of cross-coupled inverters to maintain coupling between the positive and negative paths. To equalize loading between delay cells, all delay cell signals are buffered by inverters before being used.

A dynamic logic phase detector, adapted from [23], is used in the DLL to enable high-speed operation and to avoid systematic jitter commonly associated with high-frequency bang-bang phase detectors. In measurement, the DLL was shown to lock between approximately 1.2–2.4 GHz, corresponding to $f_{\rm LO}$ between 2.4–4.8 GHz, respectively. Jitter contribution from the DLL was measured to be less than 1 ps rms.

2) LO Interpolation Network: Folding and interpolating ADCs have used resistive networks to generate multiple accurate zero crossings while minimizing the number of active components (12-bit accuracy was achieved in [24]). To generate accurate and finely separated LO phases, a two-level resistive interpolation network, shown in Fig. 6, is adapted for phase interpolation. The inputs to the interpolator are used to derive

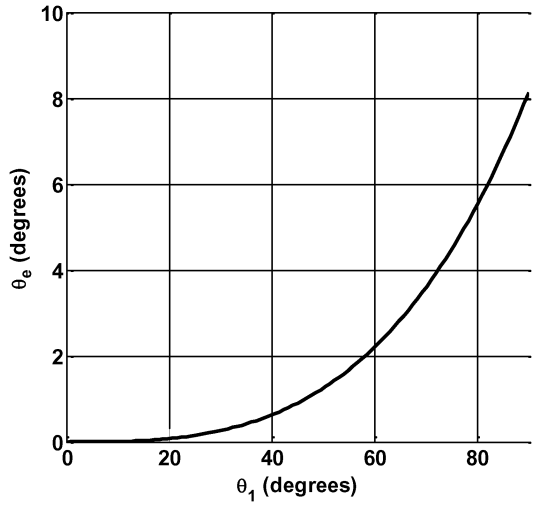

Fig. 7. Resistive interpolation phase accuracy versus input phase separation.

extra phases, and the original phases are then discarded, minimizing the amplitude-oriented phase errors between the LO signals [24]. The ends of the interpolator are cross-connected together in a ring structure to avoid edge effects and generate the output between the 0° and 157.5° phases. The interpolation network also averages out differential nonlinearity (DNL)-type phase errors from the DLL.

Resistive networks perform interpolation in amplitude, but one is used here to perform interpolation in the phase. Hence, there is a systematic interpolation phase error θ_e that must be accounted for and minimized. The phase error for sinusoidal inputs is shown in Fig. 7, where θ_e is plotted versus the phase separation between adjacent inputs to the phase interpolator (θ_1). As expected, the closer the inputs to the interpolator are to being in-phase, the more accurate the phase interpolation becomes. For example, to achieve a systematic phase error of 1°, the adjacent inputs to the phase interpolator must be no further apart than 45°. In this prototype, the input phase difference was set at 22.5°, which results in a systematic error of approximately 0.1°. Finer interpolation can be derived easily by cascading multiple interpolation networks.

Interpolator driver nonidealities and layout mismatch can also limit the achievable phase accuracy of the interpolation. Significant overlap between the interpolator input phases is needed to accurately interpolate between them. Higher order harmonics from the interpolator drivers can excessively sharpen the input transition edges, thus limiting input-phase overlap and causing additional phase error. This was addressed in simulation by ensuring that the interpolator *RC* network sufficiently filters out these harmonics. In addition, any unbalanced parasitics in the interpolation network load different sections of the network unevenly, thereby introducing frequency-dependent phase errors. It was determined during testing that the cross connection at the two ends of the interpolator introduced an unbalanced capacitance, creating an integral nonlinearity (INL)-type phase-error component that was unaccounted for in Fig. 7.

3) Edge Combiner and LO Distribution: The outputs of the phase interpolator are converted into high-frequency multiphase LO signals via a bank of edge combiners. Each edge combiner, shown in Fig. 8, performs an XOR operation on differential 0° and 90° low-frequency signals to produce a high-frequency LO signal. Pass-gate-type digital logic is used to lower parasitics, and all signals swing rail-to-rail.

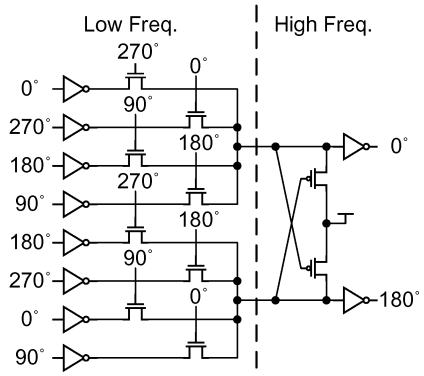

Fig. 8. Edge combiner schematic diagram.

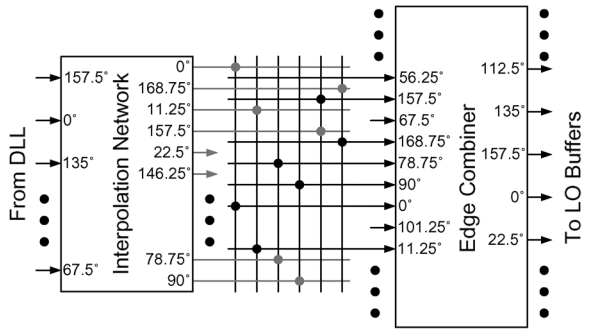

Fig. 9. LO distribution inter-stage reordering network.

Because of the large number of LO phases, a bus-type LO phase distribution layout is used. The DLL, interpolation network, and the edge combiner bank have different circuit widths and require different input and output LO phase orderings. The phase reordering network between the resistive interpolator and the edge combiners is shown in Fig. 9. All lines are differentially distributed, but a single-ended diagram is shown for simplicity. Inter-layer vias between higher level and lower level metals are denoted by junction dots. Capacitive loading on each of the lines in the reordering network is equalized over the different phases by matching all wire lengths. Coupling effects between the lines are cancelled to the first order through differential signaling and by ensuring that each LO signal line crosses every other signal line once.

B. Current-Mode Down-Conversion Channel

The circuit schematic of a single phase-shift path is shown in Fig. 10. In each path, the received signal voltage is converted to current through a resistively degenerated cascode G_m amplifier. The current is then split evenly between the passive mixers due to the uniform spacing of the LO phases between 0° and 180°, and the phase-shifting operation is performed during down-conversion. The current is then split again between the I- and Q-TIA at the outputs of the mixers and sent through a bank of passive switches to perform multiplication by b_m. The TIAs then sum together the signals to synthesize the complex gain and convert

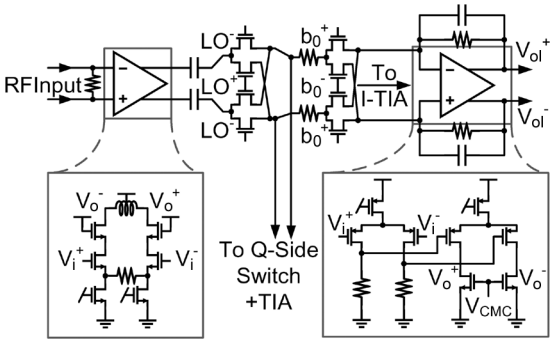

Fig. 10. Single phase-shift path circuit diagram.

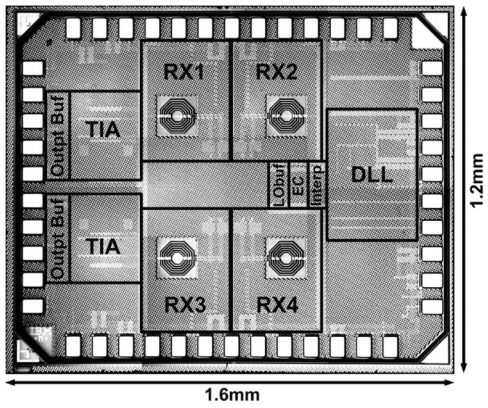

Fig. 11. Chip micrograph.

them back to voltage. Though the architecture at the top level [shown in Fig. 2(b)] may look complicated, the core components in each channel are simple.

A spiral inductor used at the G_m amplifier output acts as a choke to push current through the passive mixers and tunes out the parasitic capacitances of the amplifier and the mixer bank. The G_m amplifier input is resistively matched to 50 Ω for simplicity, but, in a full receiver, the G_m stage could be cascaded with a low-noise amplifier (LNA).

A double-balanced passive topology was chosen for the mixers. The high second-order intercept point (IIP2) and minimal flicker noise of passive mixers are important for direct-conversion architectures such as this one. The lack of static power consumption in passive mixers is also notable, given the large number of mixers in the phase-oversampling architecture.

Because the multiple LO phases that drive the mixers are not mutually orthogonal, and because the input and output of a passive mixer are shorted together for a portion of each LO cycle, an isolation problem exists between the various mixers. To properly isolate the summing nodes of the two TIAs, resistors are placed at the outputs of the mixers. The isolation resistors increase the noise figure of the channels and the voltage swing at the mixer output nodes, contributing a nonnegligible component to nonlinearity. The noise figure issue was addressed during the design phase by increasing the transconductance of the G_m stage. The linearity issue was addressed by carefully balancing the nonlinearity contributions from the G_m stage and the isolation resistor-induced voltage swings and ensuring that the latter factor does not dominate.

Signal combining between the different channels is performed at baseband to keep each channel simple and to minimize any potential coupling between them. To accomplish this, the I-TIA and Q-TIA sum together the outputs from all the mixers in the VM channels. It is advantageous for the sources and drains of the switches in the passive mixer quad to be biased close to ground to minimize their on-resistance. To accomplish this, the common mode of the second stage of the TIAs, which also sets the bias point for the passive mixers, is set to follow a low off-chip reference voltage via a common-mode feedback loop. The pMOS differential inputs are also used in the TIAs to accommodate the low input voltage.

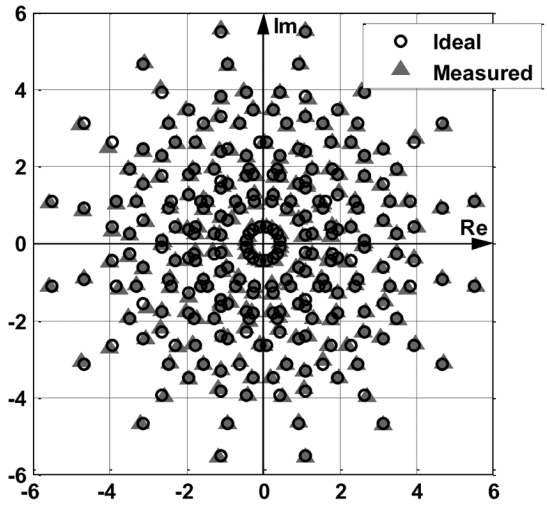

Fig. 12. Phase-oversampling VM complex gain constellation ($M = 8$).

V. Measurement Results

The test chip was implemented in a 1P8M 90-nm RF CMOS process, and the die photograph is shown in Fig. 11. The chip dimensions are 1.2 mm $\times$ 1.6 mm. All pads are ESD protected, and all core supply voltages are 1.2 V. A four-layer printed circuit board (PCB) was designed and fabricated in Rogers material for testing purposes, and chip-on-board attachment was used. The coefficients b_m and circuit tuning coefficients are scanned into the chip via a serial interface, and an field-programmable gate array (FPGA) generates the necessary control waveforms for the scan chains. During testing, one channel was first measured to determine the VM's complex gain accuracy, and then the chip was tested with two or four channels active to measure beamforming metrics.

A. Single Channel

1) Complex Gain: The complex gain for one VM channel is measured by down-converting a single RF tone and comparing the phase shift and amplitude of the device-under-test (DUT) outputs to a fixed reference tone. The complex gain is stepped through all 256 possible settings, and the data are then compiled and post-processed in MATLAB. The measured complex gain constellation of one VM channel is shown in Fig. 12.

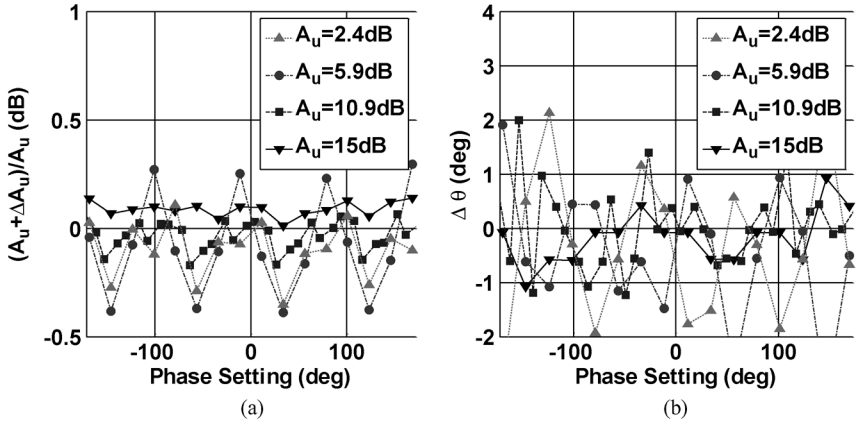

Fig. 13. (a) Complex-gain amplitude error and (b) complex-gain phase error versus different complex-gain settings.

Measured and ideal data points are shown as filled triangles and empty circles, respectively. The effects of IQ imbalance are averaged out to avoid any potential misinterpretation of the gain accuracy. The high resolution of the constellation results in a worst case measured phase error of $< 5.5^\circ$ in the gain setting, which includes both random and systematic errors (due to phase quantization), at a back-off of 4 dB from the maximum gain.

We define a metric for the complex gain accuracy, the EVM of the gain constellation, analogous to the EVM of the signal constellation used in communications, given as

$$\mathrm{EVM} = \sqrt{\frac{\sum |u - u'|^2}{\sum |u|^2}} \tag{3}$$

where u is the ideal complex gain, and u' is the measured one. For the measured complex gain shown in Fig. 12, the overall EVM of the constellation is 2%, showing good adherence to the ideal constellation.

To further elaborate on the accuracy of the complex gain and phase, complex gains u and u' are decomposed into their amplitude (A_u) and phase (θ_u) components

$$u = A_u e^{j\theta_u} \tag{4}$$

$$u\prime = (A_u + \Delta A_u) e^{j(\theta_u + \Delta\theta_u)} \tag{5}$$

where ΔA_u and $\Delta\theta_u$ are the gain and phase errors associated with the measured gain u'. Fig. 13(a) and (b) shows the relative amplitude and phase deviations of u' from u for different complex gain settings, respectively. The relative gain and phase errors in Fig. 13(a) and (b) appears larger at small gain settings than at large gain settings. The gain and phase errors are caused by static phase offsets between the multiphase LO signals, which generate an error vector that perturbs the VM's complex gain. At complex gain settings with high A_u, as shown in Fig. 14(a), this perturbation is small relative to the total gain, resulting in small $\Delta\theta_u$ and $\Delta A_u/A_u$, while in settings with low A_u, as shown in Fig. 14(b), the perturbation is large compared to the total complex gain, resulting in larger $\Delta\theta_u$ and $\Delta A_u/A_u$.

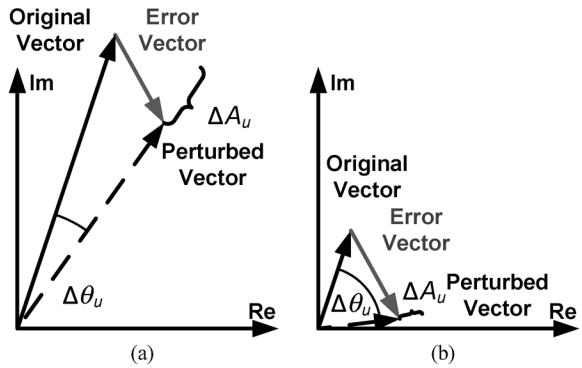

Fig. 14. LO phase error perturbation of complex gain of (a) high-gain and (b) low-gain vectors.

The magnitude and phase errors in Fig. 13(a) and (b) shows a periodic pattern across the phase settings, which is caused by a systematic component of the LO phase offsets from the resistive interpolator. The standard deviation of the LO phase offsets was deduced to be approximately 2.8° based on the measured IQ mismatch and complex gain errors. Despite the LO phase errors, the gain and phases are within 0.5 dB of the ideal magnitude, and approximately 2° to 3° of the ideal phase setting for most cases.

2) IQ Mismatch: The LO phase offsets also affect the IQ mismatch of each VM. In a single channel, the net effect of the IQ mismatch is to lower the image rejection ratio (IRR) and raise the received signal EVM. In the context of blocker cancellation via beamforming, IQ mismatch limits the achievable blocker attenuation by leaving blocker residue in the I- or Q-channel after signal combining.

The measured effects of IQ imbalance on the receiver IRR are shown in Fig. 15(a). While receiver architectures such as low-IF and Weaver require high IRR, an IRR of 20 dB can be acceptable for many direct-conversion receivers because the image is the signal itself mirrored. In this prototype, a >20-dB IRR is achieved except for the lowest gain setting shown in Fig. 15(a).

IQ matching requirements in the context of signal demodulation are more stringent. Fig. 15(b) shows the received signal EVM across different complex gain settings for a wideband OFDM signal in which each subcarrier is 64-QAM modulated.[2]

[2]Note that this plot shows signal EVM, which differs from the complex gain EVM shown earlier.

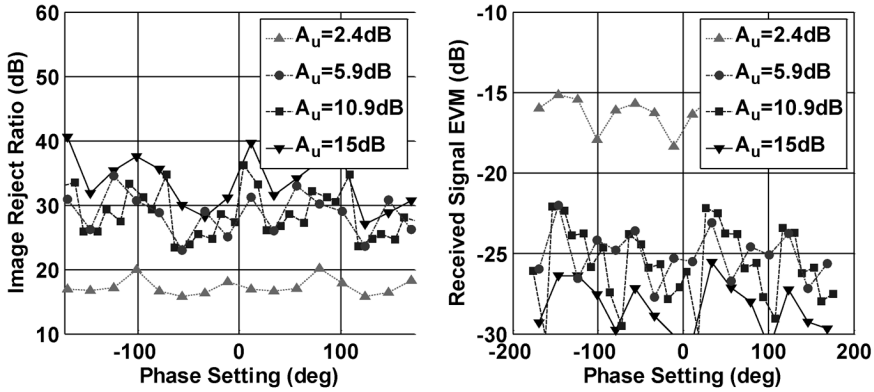

Fig. 15. (a) Image rejection ratio and (b) received signal EVM for different complex-gain settings.

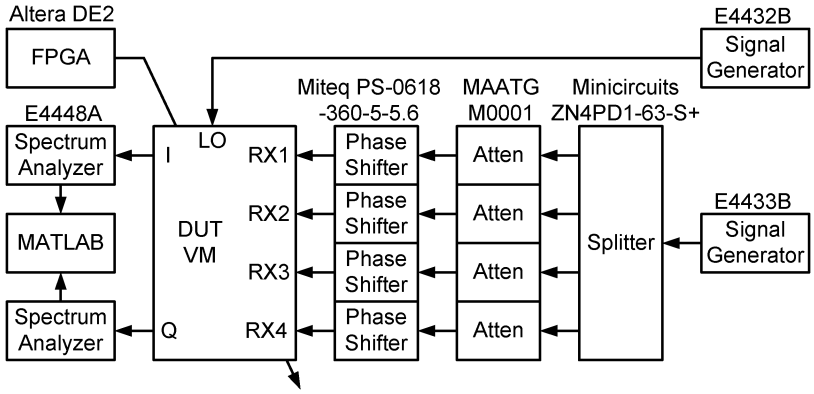

Fig. 16. Measurement setup for antenna array response.

For such signals, the maximum acceptable EVM is approximately -25 dB. This is met for the higher gain settings.

B. Multiple Channels

1) Measurement Setup: To evaluate the equivalent circuit performance in a phased array receiver, the measurement setup shown in Fig. 16 was used. A signal generator produces a single tone that is split into four paths, which are then phase-shifted via plug-in, off-chip phase shifters to mimic the effect of the signal arriving from a particular direction. Off-chip variable attenuators are used to compensate for setting-dependent gain errors in the phase shifters. The coefficients b_m for all VM channels are chosen to steer the receive beam in a particular direction. The I- and Q-outputs of the DUT are then measured across different phase-shifter settings to derive a phased-array pattern.

The measured responses of the four-channel VM receiver in phased-array mode ($d = \lambda/2$) steered to broadside and to a 60° scan angle are shown in Fig. 17(a) and (b), respectively. The dashed lines denote ideal antenna array patterns, and solid lines denote measured array patterns. The typical measured peak-to-null ratio is 20 dB. The accuracy of this measurement was limited by the gain/phase-shifting accuracies of the phase shifters and attenuators used in the experiment.

2) Interference Cancellation: An OFDM signal with 20-MHz bandwidth, in which each subcarrier is modulated via 64-QAM, is generated in MATLAB and uploaded to a signal generator. Then it is phase-shifted by off-chip components and sent into the beamformer, where it is down-converted to baseband. The DUT output is then sampled by an NI5640R PCI card to determine the effect of blockers on modulation accuracy and to demonstrate the interference cancellation of the beamformer. The spectrum of the signal at the DUT output is shown in Fig. 18(a). The signal is demodulated, and the QAM signal constellation from each subcarrier is overlaid on top of the others and shown in Fig. 18(b). Here, a large in-channel interferer is also present, limiting the signal-to-interference ratio (SIR) to 7.8 dB and the signal EVM to -8.5 dB. With a single antenna, this in-channel blocker cannot be removed, and the signal cannot be correctly demodulated.

Next, a second channel is turned on. Again, the DUT output is sampled [the spectrum is shown in Fig. 18(c)] and demodulated [the QAM signal constellation for all subcarriers is shown in Fig. 18(d)]. Both the desired signal and the in-channel blocker are phase-shifted with passive off-chip components before being input into the VMs of the down-converter, mimicking the effect of an interferer arriving from a different direction than that of the desired signal. The complex gains of the two channels are then set to actively cancel the interferer and boost the power of the desired signal. The demodulated QAM constellation is cleaned up considerably, and the received signal EVM and SIR greatly improve to -26.0 and 34.0 dB, respectively. While in-band interference cancellation has been demonstrated here, cancellation can also be used to decrease

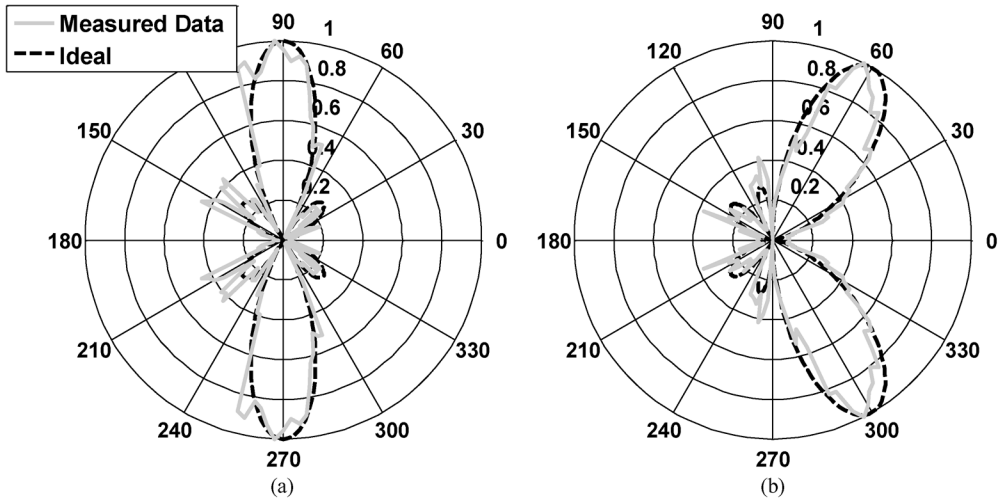

Fig. 17. Measured four-antenna array response (a) steered to broadside and (b) steered to 60°.

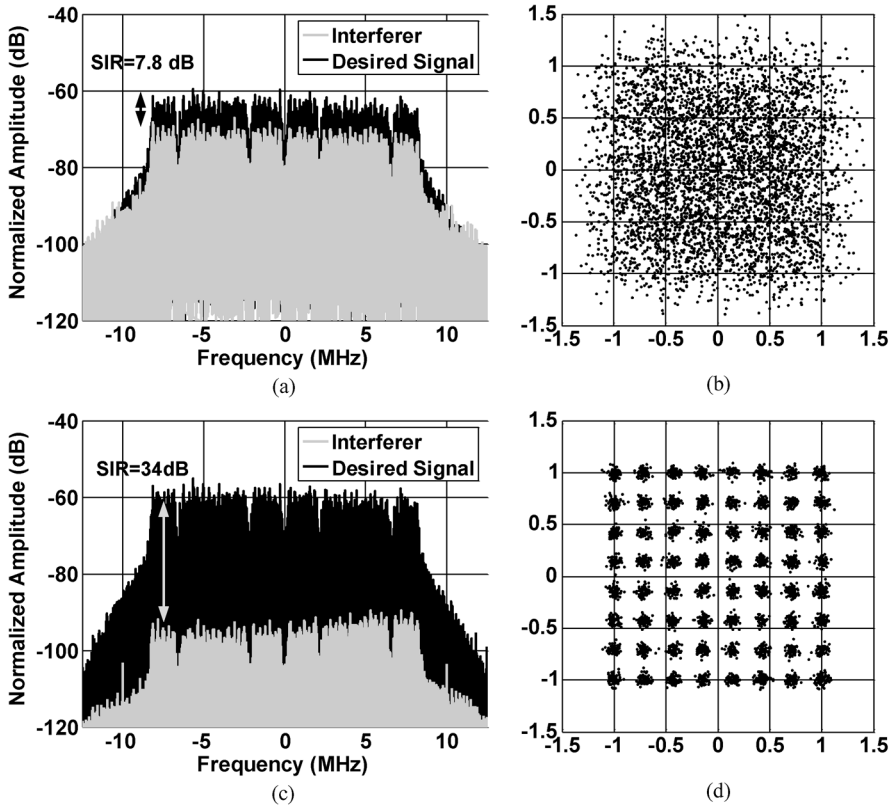

Fig. 18. In-band interference cancellation. Before interference cancellation: (a) FFT of the VM output and (b) demodulated VM output signal. After interference cancellation: (c) FFT of the VM output and (d) demodulated VM output signal.

the signal swing of blockers in neighboring channels, thereby diminishing the amount of headroom that they occupy.

In Fig. 18(c) and (d), the desired and blocker signal phase separations correspond to a difference in angle of arrival of approximately 74°. In general, a worst case in-channel blocker cancellation of $>$24 dB over all measurements was observed for blockers impinging from different directions. Achievable SIR and EVM improvements depend on the difference in angle of arrival between the desired signal and the in-channel blocker.

The effect of IQ mismatch on blocker attenuation can be analyzed by disabling the desired signal in the previous example. Fig. 19(a) and (b) shows the blocker spectra before and after cancellation, respectively. Before cancellation, the interferer amplitudes in the I- and Q-channel are approximately equal, and after cancellation, the interferer is attenuated in both the I- and Q-channel. However, the cancellation is not equal due to IQ mismatch. Note also that the frequency dependence of the IQ mismatch slightly shapes the residue in the Q-channel.

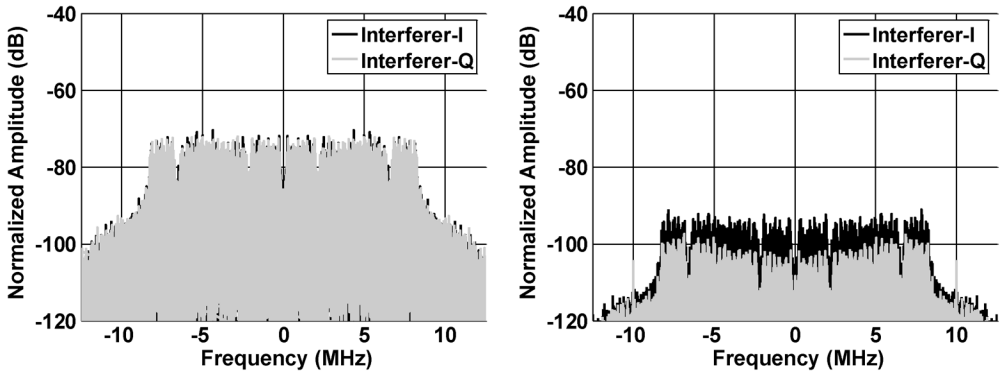

Fig. 19. Interferer I and Q channels (a) before cancellation and (b) after cancellation.

TABLE I
CMOS VECTOR MODULATORS

	[2]	[3]	[4]	This Work
Architecture	Cartesian Combining	Cartesian Combining	Cartesian Combining	Phase-Oversampling
RX Channels	4	4	2	4
Frequency	24 GHz	5 GHz	2.4 GHz	4 GHz
Max Gain	12 dB	N/A	53 dB	15 dB
NF	7.5 dB	N/A	4 dB	13 dB
IIP3	-12.5 dBm	N/A	-14 dBm	2 dBm
IIP2	N/A	N/A	N/A	45 dBm
Core Area	3.02 mm^2	4.11 mm^2	0.29 mm^2	1.92 mm^2
Supply Voltage	1.5 V	1.4 V	1.2 V	1.2 V
Technology	130 nm	90 nm	130 nm	90 nm
Typical Signal EVM (OFDM)	N/A	N/A	-32 dB	-25 dB‡
Interference Cancellation (2-Channel)	N/A	> 20 dB	N/A	> 24 dB
Power	115 mW	140 mW	30 mW	166 mW

‡Higher gain settings

Table I summarizes the experimental results of the prototype chip measured at 4 GHz, which is the frequency of maximum gain. The increased power consumption is attributable to the large number of LO distribution lines, and the large G_m stage, which is needed to drive the mixers. The 166 mW consumed by the chip is broken down as follows: the DLL and LO distribution network (including the interpolator and edge combiners) consume 18 and 55 mW, respectively, and the circuits in the signal path—G_m amplifiers and TIAs—consume 81 and 12 mW, respectively, which includes all four channels. The G_m stage power consumption can be lowered by utilizing a leading LNA to lower its noise contribution, as well as by using pseudo-differential circuits to obtain a more favorable power consumption/linearity tradeoff [4]. The LO distribution power can be reduced by lowering LO swing during distribution or by moving to a superheterodyne architecture to lower the LO frequency. Note also that, while [4] utilizes a Cartesian-combining topology, the VM (after the LNA) achieves IIP3 $>$13 dBm. We believe that the linearity in the phase-oversampling approach can be improved by utilizing a pseudo-differential signal path and through further optimization of the signal swings at the mixer outputs.

VI. CONCLUSION

A new architecture for VMs based on phase-oversampling and coarse quantization is introduced, and a four-channel beamforming IC based on the proposed VM is demonstrated. The VM prototype IC achieves accurate analog-domain phase shifting, gain control, beamsteering, and cancellation of near-channel and in-channel blockers without the use of fine-resolution RFVGAs in the signal paths. This architecture allows for the design of potentially more linear beamformers that do not need dedicated linear amplification or beamforming blocks, making it a useful candidate for multi-channel receivers in deeply scaled CMOS.

ACKNOWLEDGMENT

The authors would like to thank D. Mast for his support during testing and DARPA TAPO for chip fabrication.

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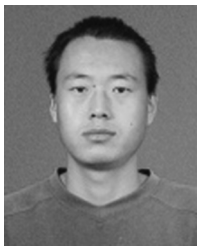

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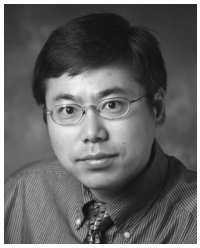

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