On-wafer DC, S-parameter and noise parameter tests were performed after the backside process. Typical V_p variation by this dry process was < 7% (< 50mV), while that by the wet recess was 20% (< 140mV). Typical measured F_{min} (minimum noise figure) at 10 and 18GHz was ~0.63 and 1.1dB with an associated gain of 15.8 and 12dB, respectively. These values were slightly better or as good as the data obtained from the wet etched devices, which demonstrates the low damage nature of our dry recess process.

LNA design: Design specifications of the X-band LNA are as follows: (i) $NF \leq 1.6$dB, (ii) gain ≥ 22dB, (iii) chip size ≤ 1mm², (iv) DC power consumption ≤ 100mW. A schematic diagram of the LNA circuit is shown in Fig. 1. Two stages instead of three were chosen for chip size and DC power considerations. A gate width of 160μm was selected for input and output matching considerations. For the input match, there was a good compromise between DC power consumption and chip size; larger devices allow simple input matching topology consisting only of a shunt inductor (Lp1 and Lp2 in Fig. 1) and thus smaller chip size, but they consume more DC power. To match 160μm PHEMTs at the input, a small series inductor (L_{s1} and L_{s2} in Fig. 1) was added to a shunt inductor. The size of this series inductor was < 0.025mm² and did not significantly increase the chip size. The input matching circuit for the first-stage transistor was designed for minimum noise figure, while that for the second-stage was designed for gain. Under these input matching conditions, the output impedance of the 160μm PHEMT was close to 50Ω. No output matching circuitry was required to achieve better than 10dB output return loss, simplifying the circuit and reducing the chip size.

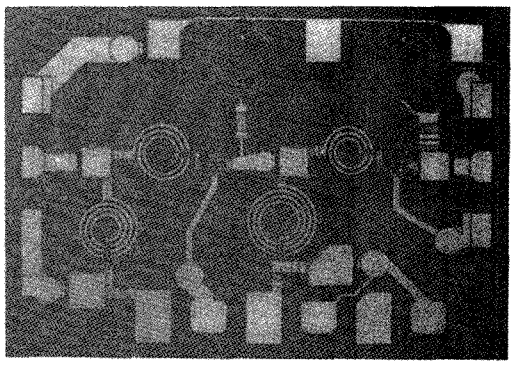

Fig. 2 *Photograph of X-band MMIC LNA*

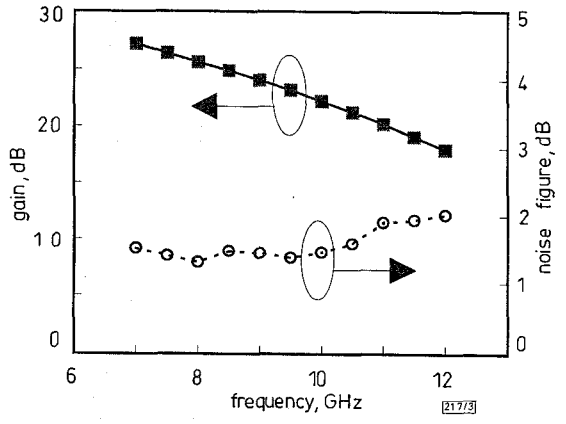

Fig. 3 *Measured gain and noise figure of X-band LNA under low-noise bias conditions*

($I_{ds} = 0.2 \times I_{dss}$)

To maximise the gain while keeping NF small, different drain biases were applied at each stage. First-stage drain bias was set to 1.2V for low noise, and the second-stage bias was 2.2V for high gain. The on-chip resistive voltage divider was used for this purpose (R1 and R2 in Fig. 1). Series inductive feedback was added at the source end for simultaneous noise and power match. High impedance lines were used for this feedback. All the biasing networks were included on-chip. Also included on-chip were the DC probe pads which allow fast automatic on-wafer testing without worrying about low frequency oscillation problems. A photograph of the LNA chip is shown in Fig. 2. The chip size was 1mm² including the probe pads and 0.9mm² without the DC probe pads. The chip size can, however, be easily reduced by at least 20% through more compact design which was not carried out in this first pass design.

Measured results: Measured frequency dependence of gain and noise figure is shown in Fig. 3. Low-noise bias conditions were used for this measurement; the common drain bias voltage (V_{dd} in Fig. 1) was set to 2.5V and total current was 30mA ($0.2 \times I_{dss}$). The total DC power consumption was thus ~75mW. The circuit exhibited better than 2dB noise figure over the whole measurement range of 7–12GHz. The measured noise figure at 10GHz was ~1.45dB, and the corresponding gain was ~22dB.

The uniformity of the chip was also tested by measuring the gain of the circuits from three different wafers under fixed bias conditions. An automatic probe station was used for this purpose, and high-gain bias conditions (P_{dc} = 90mW) were applied. The average gain at 10GHz was ~23dB and the standard deviation was ~0.9dB, which demonstrates the good uniformity of our dry recess process.

Conclusion: In this work, dry recessed PHEMTs were used to implement compact/low-DC power LNAs at X-band. A high gain design allowed compact two-stage amplifiers with better than 22dB gain at 10GHz. The corresponding noise figure was < 1.5dB. The selective recess process resulted in uniform characteristics without source bias resistors. The DC power consumption and the chip size were reduced thanks to optimum circuit design and the absence of source resistors. This work demonstrates that, with proper circuit design and dry recess technology, highly-manufacturable ultralow-noise amplifiers are possible with low DC power consumption and small chip area.

7 February 1997
Electronics Letters Online No: 19970544

Y. Kwon (*School of Electrical Engineering, Seoul National University, San 56-1 Shilim-Dong, Kwanak-Ku, Seoul, South Korea*)

E.A. Sovero, D.S. Deakin and J.A. Higgins (*Rockwell Science Center, Thousand Oaks, CA 91360, USA*)

References

1 LOTT, U.: 'Low DC power monolithic low noise amplifier for wireless applications at 5GHz'. Proc. IEEE Microw. Millimeter-wave Monolithic Circuits Symp., 1996, pp. 81–84

2 SHIGA, N., NAKAJIMA, S., KUWATA, N., OTOBE, K., SEKIGUCHI, T., MATSUZAKI, K., and HAYASHI, H.: 'Monolithic pulse-doped MESFET LNA for DBS downconverter'. Proc. GaAs IC Symp., 1992, pp. 127–130

3 HUGHES, B., PERDOMO, J., and KONDO, H.: '12GHz low-noise MMIC amplifier designed with a noise model that scales with MODFET size and bias', *IEEE Trans. Microw. Theory Tech.*, 1993, **41**, pp. 2311–2316

4 KWON, Y., DEAKIN, D.S., SOVERO, E.A., and HIGGINS, J.A.: 'High-performance Ka-band monolithic low-noise amplifiers using 0.2μm dry-recessed GaAs PHEMTs', *IEEE Microw. Guid. Wave Lett.*, 1996, **6**, pp. 253–255

Near-infrared wavelength intersubband transitions in high indium content InGaAs/AlAs quantum wells grown on GaAs

B. Sung, H.C. Chui, M.M. Fejer and J.S. Harris, Jr.

Indexing terms: Semiconductor quantum wells, Gallium arsenide

The authors report intersubband transitions shorter than 2 μm in square and coupled InGaAs/AlAs quantum wells (QWs) grown on GaAs substrates. The linearly graded buffer technique is used to facilitate the growth of quantum wells with indium contents of 50 and 60%. E_{12} of 720meV (1.72μm) is achieved in six monolayer (ML) wide $In_{0.6}Ga_{0.4}As$/AlAs QWs. Asymmetrically coupled $In_{0.5}Ga_{0.5}As$/AlAs QWs exhibit intersubband transition as high as 780meV (1.59μm) for the 1–4 transition.

Intersubband transitions in the conduction band of a quantum well (QW) have been widely studied for applications to photodetectors, modulators, nonlinear optics and mid-infrared lasers [1, 2]. However, these applications have been restricted to long wavelengths (>4μm) in conventional GaAs/AlGaAs QWs; there has been much effort to increase the intersubband energy so as to extend their application to shorter wavelengths. InGaAs/AlAs QWs have been the materials of choice for short wavelength intersubband transitions because of their large conduction band discontinuity. Recently, near-infrared wavelength (1.55μm, 1.9μm) intersubband transitions have been reported in InGaAs/AlAs QWs on InP and GaAs substrates [3, 4]. However, lattice mismatch between the well and barrier materials limits the indium content and number of QWs that can be grown without significant material degradation. Indium composition in QWs was restricted to < 40% for a GaAs substrate [4] and the number of QWs was no more than two periods for $In_{0.53}Ga_{0.47}As$/AlAs QWs on an InP substrate [3]. This limitation can be circumvented with a novel growth technique of growing an InGaAs buffer layer with linearly graded indium composition prior to the growth of multiple QWs (MQWs) [5]. We report here near-infrared intersubband transitions as short as 1.59μm from square and coupled InGaAs/AlAs QW samples where indium concentrations of 50 and 60% were successfully incorporated into > 100 MQW layers via strain accommodation in epi-layers facilitated by a graded buffer.

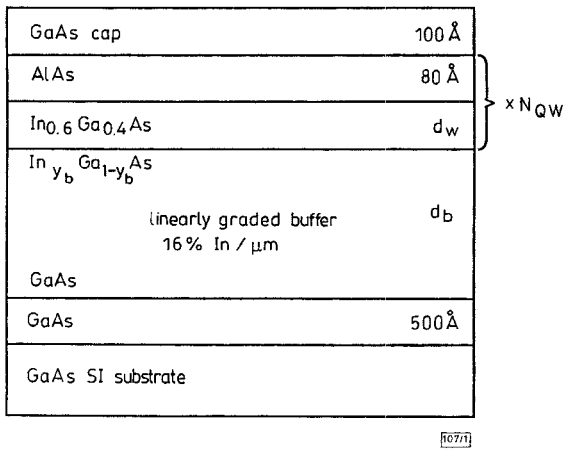

Fig. 1 *Layer structure of square QW sample*

N_{QW} = 188, 214, 250 for d_W = 22.6, 19.8, 17.0Å, respectively
Final buffer indium composition y_b is 0.2 and buffer layer thickness d_b is 12500Å

Fig. 1 shows the layer structure of an $In_{0.6}Ga_{0.4}As$/AlAs square MQW sample. A detailed growth procedure and optimisation of growth parameters for high quality InGaAs/AlGaAs QWs have been presented elsewhere [6]. All samples were grown by molecular beam epitaxy on semi-insulating GaAs substrates. Growth started with a 500Å GaAs layer and then a thick $In_yGa_{1-y}As$ graded buffer layer was deposited with indium composition, y, linearly graded at a rate of 16%/μm up to the final composition, y_b = 0.2. The final buffer layer serves as an effective substrate with an intermediate lattice constant to give strain compensation to both the well and barrier layers. Three $In_{0.6}Ga_{0.4}As$/AlAs MQW samples were grown with well widths d_w = 22.6, 19.8, and 17.0Å which correspond to 8, 7, and 6 monolayers (MLs), respectively. The barrier width between the wells is 80Å. They were uniformly doped n-type in the well region to $n = 3 \times 10^{18}cm^{-3}$. The number of QWs increased with decreasing well width, N_{QW} = 188, 214, and 250, respectively, to have approximately the same total sheet carrier density.

Near-infrared absorption spectra were taken on these samples at room temperature using a Fourier transform infrared spectrometer with a tungsten lamp and a InSb detector. Two end facets ~6.5mm long samples were polished at 45° so that light incident normal to a polished facet passed through the MQW layers ~16 times to enhance the QW intersubband absorption. Reference samples taken from the same wafers were proton implanted to eliminate the free electrons in the wells; light transmission through the samples was normalised by these reference samples. A side view of the sample showing the configuration for TM and TE polarised light is shown in the inset of Fig. 2. The absorbance data in Fig. 2 are for TM polarisation. We observed no intersubband absorption for TE polarised light unlike previous reports [3]. E_{12} is 667 (639) meV, 694 (699) meV, and 720 (758) meV for d_w = 22.6, 19.8, and 17.0Å, respectively. Numbers in parentheses are theoretical values based on an energy dependent effective mass approximation [7]. The integrated absorption fraction decreases rapidly with decreasing width of the QW.

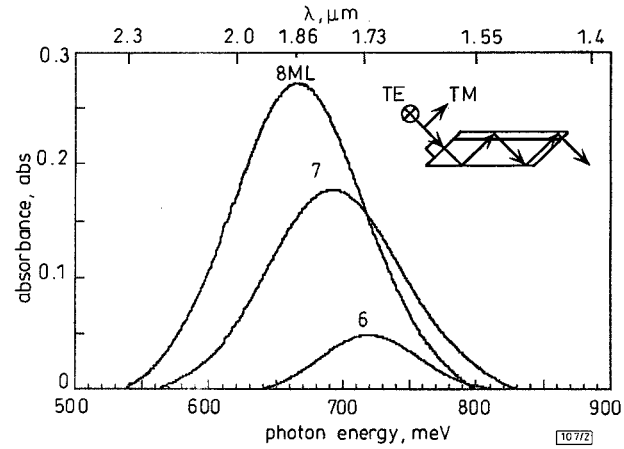

Fig. 2 *Intersubband absorption spectra from three $In_{0.6}Ga_{0.4}As$/AlAs square QW samples*

d_W = 22.6Å (8 ML), 19.8Å (7 ML), 17.0Å (6 ML)
Peak energy of 6ML wide QW sample corresponds to 1.72μm
Inset: side view of sample showing configuration for TM and TE polarisation of incident light
Absorbance data are for TM polarisation

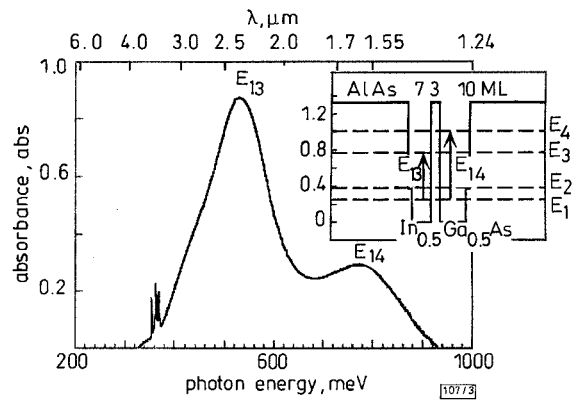

Fig. 3 *1–3 and 1–4 absorption spectra for coupled $In_{0.5}Ga_{0.5}As$/AlAs QW sample*

1–2 transition is not shown here
E_{13} and E_{14} correspond to 2.34 and 1.59μm, respectively
Inset: structure of coupled QW, 7 and 10 ML QWs coupled by 3 ML wide AlAs layer
GaAs single MLs are deposited on left and right boundaries between wells and barriers

To obtain a higher intersubband energy without further reduction of QW width, we measured a coupled QW sample. This sample contains 100 coupled QWs, each coupled QW consisting of 10 and 7 ML $In_{0.5}Ga_{0.5}As$ QWs separated by a 3 ML thick AlAs layer as shown in the inset of Fig. 3. GaAs single MLs were deposited on each boundary between the wells and barriers to smooth the interface [6]. These MQW layers are atop an InGaAs buffer layer with y_b = 0.25. The QWs are highly n-type doped to $n = 10^{19}cm^{-3}$. Strong absorption peaks were observed from 1–3 and 1–4 transitions as shown in Fig. 3. There is a 1–2 absorption peak at 142 meV which is not shown in Fig. 3. The 1–3 and 1–4 transition energies are 530 mev (2.34μm) and 780meV (1.59μm), respectively. The two peaks are not completely separated because of their large linewidths. Even considering the high doping concentration in the QWs, the integrated absorption fractions for 1–3 and 1–4 transitions are greater than those of the previous square QW samples shown in Fig. 2. A coupled QW can be designed to have 1–3 and 1–4 oscillator strengths comparable to a 1–2 transition, which is not possible in a square QW where the 1–3 transition is forbidden and 1–4 transition is weaker than 1–2 transition by about two

orders of magnitude. This makes the 1–3 or 1–4 transitions in a coupled QW promising for near-infrared applications.

In summary, we have observed near-infrared wavelength intersubband transitions as short as 1.59μm in high indium content InGaAs/AlAs QWs on a linearly graded InGaAs buffer. 1–3 and 1–4 transitions in a coupled QW were as strong as the 1–2 transition in a narrow square QW at comparable transition energies. QW photodetectors, modulator and nonlinear optics applications operated at near-infrared wavelengths (1.55–2.00μm) should be possible using these materials.

Acknowledgment: B. Sung thanks G.L. Woods for helpful discussions and F. Sugihwo for his help in sample preparation. This work was supported by DARPA and ONR through the Center for Non-linear Optical Materials at Stanford, contract N00014-92-J-1903.

30 January 1997
Electronics Letters Online No: 19970514

B. Sung and J.S. Harris Jr. (*Solid State Laboratory, CIS-X, Stanford University, Stanford, CA 94305, USA*)

H.C. Chui (*Ginzton Laboratory, Stanford University, Stanford, CA 94305, USA*)

M.M. Fejer (*Hewlett-Packard Optoelectronics Division, 350-370 W. Trimble Road, San Jose, CA 95131, USA*)

References

1 LIU, H.C., LEVINE, B.F., and ANDERSSON, J.Y. (Eds.): 'Quantum well intersubband transition physics and devices' (Kluwer Academic Publishers, Dordrecht/Boston/London), 1994

2 FAIST, J., CAPASSO, F., SIVCO, D.L., SIRTORI, C., HUTCHINSON, A.L., and CHO, A.Y.: 'Quantum cascade laser', *Science*, 1994, **264**, pp. 553–556

3 SMET, J.H., PENG, L.H., HIRAYAMA, Y., and FONSTAD, C.G.: 'Electron intersubband transitions to 0.8eV (1.55μm) in InGaAslAlAs single quantum wells', *Appl. Phys. Lett.*, 1994, **64**, pp. 986–987

4 ASANO, T., NODA, S., ABE, T., and SASAKI, A.: 'Near-infrared intersubband transitions in InGaAs/AlAs quantum wells on GaAs substrate', *Jpn. J. Appl. Phys.*, 1996, **35**, pp. 1285–1291

5 LORD, S.M., PEZESHKI, B., and HARRIS, J.S., Jr.: 'Investigation of high In content InGaAs quantum wells grown on GaAs by molecular beam epitaxy', *Electron. Lett.*, 1992, **28**, pp. 1193–1195

6 CHUI, H.C., and HARRIS, J.S., Jr.: 'Growth studies of $In_{0.5}Ga_{0.5}As$/AlGaAs quantum wells grown on GaAs with a linearly graded InGaAs buffer', *J. Vac. Sci. Tech. B*, 1994, **12**, pp. 1019–1022

7 CHUI, H.C., MARTINET, E.L., FEJER, M.M., and HARRIS, J.S., Jr.: 'Short wavelength intersubband transitions in InGaAs/AlGaAs quantum wells grown on GaAs', *Appl. Phys. Lett.*, 1994, **64**, pp. 736–738

Noise modelling of dual-gate MESFET

V. Marković, B. Milovanović and N. Maleš-Ilić

Indexing terms: MESFET, Semiconductor device noise, Semiconductor device models

A dual-gate MESFET noise model, based on two cascaded single-gate MESFET intrinsic equivalent circuits, is proposed. Four assigned equivalent temperatures are extracted together with the other model elements. A CAD oriented procedure is developed for the determination of dual-gate MESFET noise parameters over a wide frequency range.

Introduction: The ability of the automatic gain control of the dual-gate MESFET (DG-MESFET) is particularly valuable for the receiver input amplifier, which may have to accommodate a large range of RF input levels. Several DG-MESFET small-signal models have been proposed [1, 2]. However, to the authors' knowledge, the published models do not include any elements which represent the noise characteristics. In addition, the standard commercial programs for microwave circuit design do not contain DG-MESFET noise models. The goal of this Letter is to obtain a model which can predict the signal as well as the noise behaviour; this would be convenient for incorporation into microwave circuit simulators.

In [3], the authors developed a CAD-oriented procedure for obtaining the noise parameters of a single-gate MESFET based on Pospieszalski's model [4]. Here, a procedure for DG-MESFET signal and noise modelling is developed, using the standard commercial microwave circuit simulator Libra [5] which is available to most microwave circuit designers.

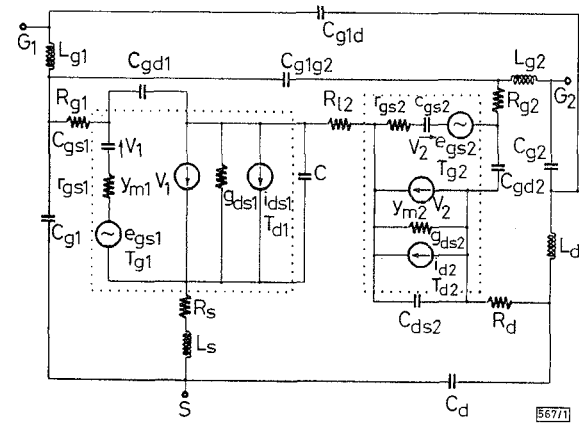

Fig. 1 *DG-MESFET noise equivalent circuit*

DG-MESFET equivalent circuit including noise sources: The DG-MESFET is considered as the cascade of two standard MESFETs. By replacing each part by its small-signal equivalent circuit and connecting them, a complex equivalent circuit is formed. The noise modelling is achieved by incorporating the noise sources, in a similar way as for a single-gate MESFET [3]. Namely, a gate noise voltage and a drain noise current are assigned to each intrinsic part of the composed equivalent circuit. The complete signal and noise model with four noise sources e_{gs1}, i_{ds1}, e_{gs2} and i_{ds2} is shown in Fig. 1, where the intrinsic circuits are denoted by dotted boxes. The effect of the noise sources is expressed through appropriate equivalent noise temperatures T_{g1}, T_{d1}, T_{g2} and T_{d2}, respectively, in the following way:

$$\langle |e_{gs1,2}|^2 \rangle = 4kBr_{gs1,2}T_{g1,2} \quad (1)$$

$$\langle |i_{ds1,2}|^2 \rangle = 4kBg_{ds1,2}T_{d1,2} \quad (2)$$

where k is the Boltzmann constant, B the incremental bandwidth and $\langle\ \rangle$ indicates the time average.

Starting from the admittance noise representation and assuming that the correlation between the noise voltage source and noise current source is negligible, the expressions for the noise parameters of a single-gate MESFET intrinsic circuit are derived [4]. On the basis of this, the noise parameters for each of two intrinsic circuits of the DG-MESFET are formulated here. Namely, minimum noise figure $F_{min1,2}$, optimum source impedance $Z_{opt1,2}$ corresponding optimum reflection coefficient $\Gamma_{opt1,2}$ (Z_0 is reference impedance) and equivalent noise resistance $R_{n1,2}$ are expressed as the functions of circuit elements and equivalent temperatures:

$$F_{min1,2} = 10\log\left[2\frac{\omega C_{gs1,2}}{g_{m1,2}T_o} \times \sqrt{r_{gs1,2}g_{ds1,2}T_{g1,2}T_{d1,2} + \left(\frac{\omega C_{gs1,2}r_{gs1,2}g_{ds1,2}T_{d1,2}}{g_{m1,2}}\right)^2} + \frac{2\omega^2 C_{gs1,2}^2 r_{gs1,2}g_{ds1,2}T_{d1,2}}{g_{m1,2}^2 T_o} + 1\right] \quad (3)$$

$$Z_{opt1,2} = \sqrt{\left(\frac{g_{m1,2}}{\omega C_{gs1,2}}\right)^2 \frac{r_{gs1,2}T_{g1,2}}{g_{ds1,2}T_{d1,2}} + r_{gs1,2}^2} + j\frac{1}{\omega C_{gs1,2}} \quad (4)$$

$$\Gamma_{opt1,2} = (Z_{opt1,2} - Z_0)/(Z_{opt1,2} + Z_0) \quad (5)$$

$$R_{n1,2} = \frac{T_{g1,2}}{T_o}r_{gs1,2} + \frac{T_{d1,2}g_{ds1,2}}{T_o g_{m1,2}^2}(1 + \omega^2 C_{gs1,2}^2 r_{gs1,2}^2) \quad (6)$$

The model elements are extracted using the powerful optimising possibilities of program Libra. The procedure includes the following steps: first, the noise parameter values obtained by eqns. 3 – 6