

Ultrafast Sampling using Low Temperature Grown GaAs MSM Switches Integrated with CMOS Amplifier for Photonic A/D Conversion

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Within the past few years, various photonic A/D conversion systems have achieved speed and resolution performance far surpassing conventional mixed signal technology, lending merit to this hybrid approach [1,2]. In our system, we utilize an optically triggered, electrical sample and hold scheme with low temperature (LT) grown GaAs MSM switches. The switch is attached to a transmission line and samples the input electrical signal onto a hold capacitor when optically activated by a short-pulse laser. An electrical A/D converter then digitizes the held signal. By time-interleaving a number of these channels, the aggregate sampling rate of the system is increased, with the larger bandwidth requirements being placed on the input sample and hold. The short carrier trapping time and relatively high mobility of the LT GaAs material provide broadband sampling capability with good optical sensitivity [3].

Previously, we demonstrated a sample and hold test circuit with 5.7 effective number of bits (ENOB) accuracy under dc input conditions and a sampling gate width of less than 2 ps [4]. The sample and hold process exhibits good linearity for up to 20 GHz input frequency and a >50 GHz 3 dB bandwidth [5].

In this work, we demonstrate LT GaAs MSM switches integrated with the front-end silicon-CMOS buffer amplifier stage with linear sampling capability from dc to 20 GHz input frequency. To our knowledge, this represents the highest bandwidth of any integrated system with CMOS technology.

MSM switches were made by depositing titanium/gold contact metal on a LT GaAs epitaxial-layer, grown at 250°C substrate temperature and post-growth annealed at 700°C for 1 minute. The CMOS circuit was fabricated in a National Semiconductor 0.24 μm technology. MSMs were integrated to the CMOS chip using a flip-chip bonding technique using indium solder bumps. Fig. 1 shows a schematic of the circuit. An 80 MHz repetition rate titanium/sapphire mode-locked laser triggers MSM1 with a ~ 150 fs FWHM, 60 pJ optical pulse, closing the switch and sampling the input voltage signal onto input1. The hold capacitance (C_{H1} , C_{H2}) is the sum of the amplifier input gate capacitance (~ 20 fF) and the substrate capacitance. Identical to MSM1, MSM2 allows input2 to track the capacitive feedthrough signal caused by variation in the input signal. Differential detection eliminates this feedthrough fluctuation. PMOS buffers, followed by a differential pair amplify the signal. The amplifier was designed with a 1 GHz 3 dB bandwidth with the 200 fF load of the eventual A/D converter, verified with SPICE simulation. High-impedance, high-speed probes were connected to the amplifier outputs, allowing oscilloscope detection with proper output common-mode biasing. Output signal response is largely determined by the output pole of the amplifier, due to the large capacitive load from the chip package (~ 4 pF) and probes (2 pF).

For low frequency testing, 5 ns wide electrical pulses phase-locked to the optical pulse train were sampled. The lower voltage of the signal was set to the nominal input common-mode value (ground), the upper voltage of the pulse being varied. Electrical pulse repetition rate was divided to $1/64^{\text{th}}$ of the optical pulse repetition rate to allow one optical pulse to sample the upper voltage, and 63 subsequent optical pulses to reset input1 back to ground. Fig. 2 shows the oscilloscope output. The initial rising edge of the signal corresponds to a single optical pulse charging the hold capacitor. A time constant of ~ 3.2 ns is observed, in good agreement with the 600 Ohm load resistance and the load capacitance mentioned above. The falling edges show subsequent pulses resetting the input. The consistent exponential shape of the edges verifies the process is a linear, single pole response to first-order. The magnitude of the rising edge is thus, proportional to the differential output voltage the amplifier would eventually settle to. The rising edge magnitude as a function of input electrical pulse amplitude is shown in Fig. 3. Linearity of the plot confirms sample and hold accuracy for the input voltage range used (6.8 ENOB).

To characterize linearity for higher input frequencies, phase-locked RF sinusoids were generated using the laser trigger and frequency multipliers. Using a mixer, this signal was then modulated by the same electrical pulse signal as above. The first optical pulse samples the RF signal and subsequent pulses reset the input, resulting in an output waveform similar to Fig. 2. By varying the phase of the RF source, different points of the sinusoid are sampled with a corresponding change seen in rising edge magnitude. Due to mixer leakage, the input was reset to $\sim 5\%$ of the input signal value, introducing a deterministic memory effect to the held signal. This effect was reflected in fluctuation of

the baseline value of the waveform as the input signal phase was changed. The rising edge magnitude as a function of phase delay is shown in Fig. 4 for 10 GHz and 20 GHz inputs (~2 Volts peak-to-peak). Dots indicate sampled points with solid lines showing pure sinusoids fit to data using a minimum mean squared error fit. Good fit confirms the linearity of the sampling process. We believe accuracy is limited by distortion of the original signal and fluctuation of the phase delay mechanism.

In conclusion, we have demonstrated an integrated sample and hold circuit with LT GaAs MSM switches flip-chip bonded to a CMOS amplifier. Measurement results show accurate, linear sampling from dc to 20 GHz input, confirming wideband sampling capability.

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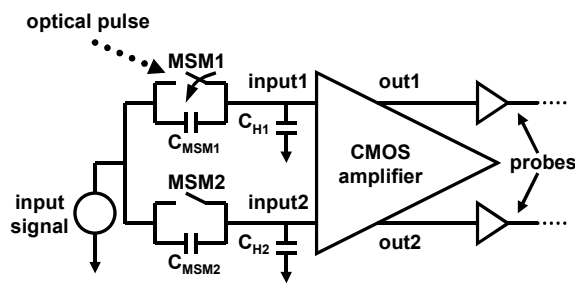


Fig. 1. Schematic of experimental setup. MSM1 is optically triggered, sampling the input signal onto input1. $C_{MSM1} = C_{MSM2}$ and $C_{H1} = C_{H2}$, allowing differential detection to eliminate feedthrough noise.

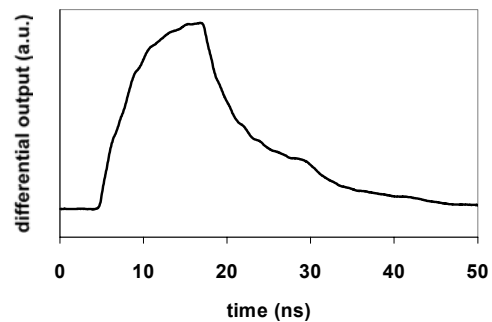


Fig. 2. Differential output of amplifier. Rising edge indicates single optical pulse sampling input signal. Subsequent pulses discharge hold capacitor (C_{H1}).

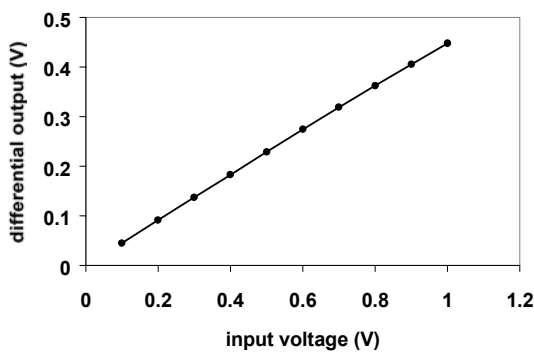


Fig. 3. Rising edge magnitude as a function of sampled voltage (low frequency input). Linearity verifies sample and hold accuracy for 1 volt range (6.8 ENOB).

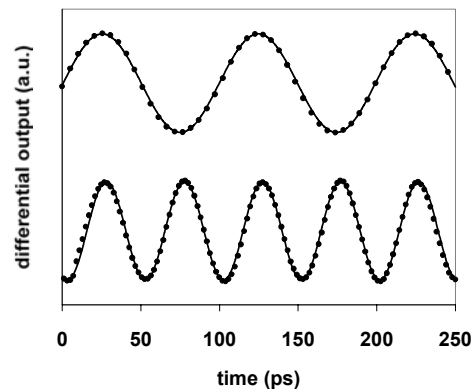


Fig. 4. Results of 10 and 20 GHz input sinusoid sampling. Dots indicate sampled points, with solid lines showing pure sinusoids fit to data.