

# Optical Pump-Probe Latency Measurements of Silicon CMOS Optical Interconnects

Gordon A. Keeler, Diwakar Agarwal, Christof Debaes<sup>†</sup>, Bianca E. Nelson,  
Noah C. Helman, and David A. B. Miller

*Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305-4085*

*Tel: (650) 725-2291, email: gkeeler@stanford.edu*

<sup>†</sup>*Permanent Address: Department of Applied Physics and Photonics, Vrije Universiteit Brussel, Brussels, Belgium*

**Abstract** – We present the first measurements of O/E/O conversion latency in a hybridly-integrated optoelectronic/CMOS chip designed for chip-to-chip optical interconnection. Using an optical pump-probe technique, we perform precise measurements with picosecond resolution that closely match our simulations.

Optical interconnects have the ability to alleviate the looming CMOS interconnect bottleneck by providing extremely dense, high-bandwidth links in chip-to-chip and, potentially, on-chip applications. While many of the advantages of an optical approach have been demonstrated experimentally, an important parameter that has not yet been properly characterized is the signal delay, or interconnect latency. If optics is to displace wiring in on-chip and chip-to-chip links, the signal latency of optical interconnects must be comparable to or lower than that of the electrical interconnects they replace.

We can separate the signal delay of an optical link into three components: transmitter latency, time-of-flight latency, and receiver latency. Since the time-of-flight delay is simple to calculate and entirely system dependent, we are most interested in measuring the electrical-to-optical (transmitter) and optical-to-electrical (receiver) constituents. Due to the inherent speed limitations of silicon CMOS and the capacitive loading effects of electrical probing, precise measurement of these short delays is difficult using electronics. Thus we use an optical technique and consider the two delays together, performing a measurement of the O/E/O conversion latency using an electrically back-to-back receiver/transmitter pair. A simplified schematic of the O/E/O circuit used for latency measurements is shown in Figure 1.

The circuits used in this experiment were fabricated in 0.25  $\mu\text{m}$  silicon CMOS using a transimpedance-amplifier-based receiver design. The receivers and transmitter drivers are inverter based and optically differential, designed for gigabit/second operation with small areas and low power consumption. To improve speed and channel density, the optoelectronic I/O devices were integrated to the CMOS in arrays via flip-chip bonding. The devices are MBE-grown GaAs multiple-quantum-well p-i-n diodes that serve as modulators and photodiodes. They have a pitch of 62.5  $\mu\text{m}$  x 125  $\mu\text{m}$  and a capacitance of roughly 250 fF after integration.

The experiment was performed in an optical pump-probe setup, using the  $\sim 100$  fs pulses from a modelocked Ti:sapphire laser with a wavelength of 850 nm. Figure 2 shows a conceptual layout. The differential input data is comprised of a repetitive optical pulse train (pump beam) and a cw diode laser (balance beam), both incident on the detector pair of the receiver. The voltage at the transmitter modulator is optically sampled with a readout pulse (probe beam). By varying the delay between the pump and probe, the temporal response of the optoelectronic circuit was mapped with picosecond resolution.

We define the latency to be the time between incidence of the input signal and the 50% transition point of the output. The observed latency of O/E/O conversion with our circuits ranges from 500-600 ps. In Figure 3(a), we compare circuit simulation results to the measured delay as a function of received energy per bit. Figure 3(b) shows simulated and experimental data for delay vs. supply voltage at a constant optical power. This variation with supply voltage is important at high clock rates, since on-chip switching noise can cause large supply variations that translate to jitter at the receiver output. In both figures the data closely matches circuit simulation results, indicating the validity of our measurements. Additional results to be presented in this talk compare the measured latency using short-pulse RZ and conventional NRZ signaling formats. We demonstrate a reduction of latency by more than 70% through the use of short pulses.

In conclusion, we have performed pump-probe measurements of optical interconnect latency on a hybridly-integrated optoelectronic/CMOS chip. This technique allows precise measurements of high-speed CMOS circuit delays down to very short time scales. When compared to the latencies predicted in future electrical interconnects [1], our findings suggest that optical interconnects can provide comparable or lower signal latency than their electrical counterparts in both chip-to-chip and on-chip applications.

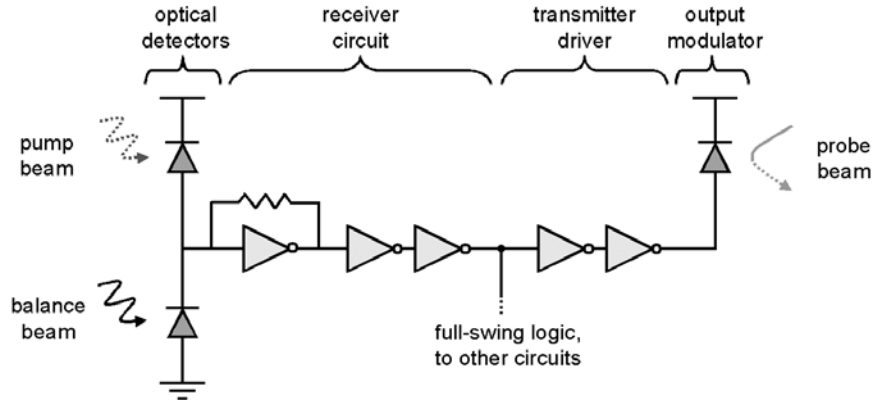


Figure 1. Simplified schematic diagram of transimpedance-based receiver and transmitter driver circuits used in latency measurements.

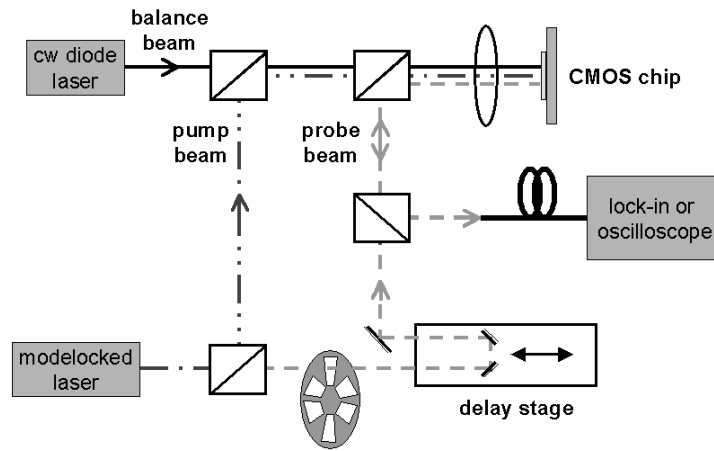


Figure 2. Schematic of the optical pump-probe setup used for interconnect latency measurements.

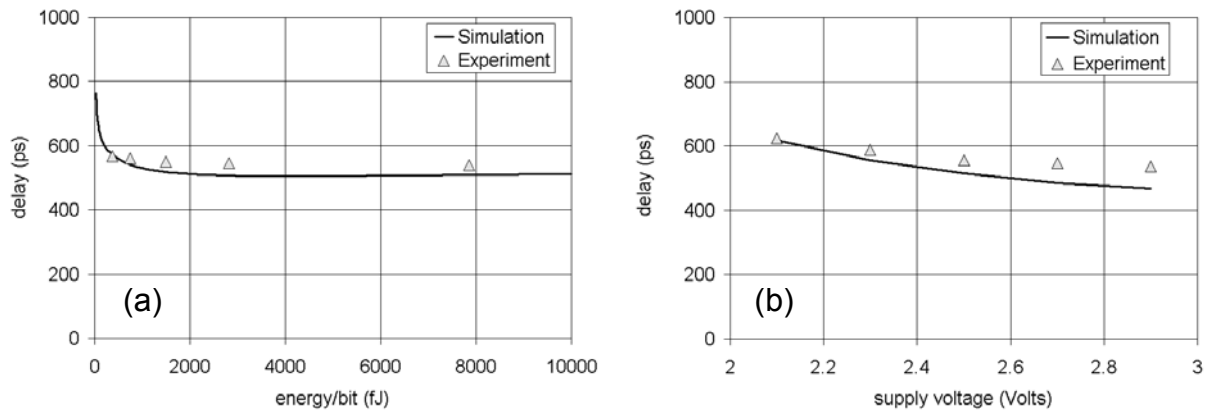


Figure 3. Simulated and measured O/E/O latency as a function of (a) received optical energy/bit using a 2.5 Volt supply, and (b) supply voltage using 1500 fJ/bit.

REFERENCES

[1] D. A. B. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," *Proc. IEEE*, **88**, 728-749 (2000).