Workshop: Metrology Beyond CMOS

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Over the past decade, researchers and technologists have become better and better at making nanoscale objects. One example of such object we don't often consider is the transistors in computer chips. There are now nearly one billion of them in each processor, each with nanoscale critical dimensions (60 nanometer gate length, several nanometer dielectric thickness.) Even more remarkably, if even a few of these transistors failed the computer would not work. Clearly, there is a great need to be able to measure local properties of today's and tomorrow's transistors, to ensure that we know what we're making and why it operates the way it does. These local properties may include structure, down to the 3-dimensional location of individual impurity atoms, local electrical conductivity, local heat flow, and even magnetic or spin properties for some future computing device concepts (and other applications).

On December 14-15, 2006, CPN co-sponsored a workshop to explore these problems. Our partners were the Center for Functional Engineered Architectonics, funded by DARPA and the Semiconductor Industry to explore materials, devices, and architectures for future computing; and the California NanoSystems Institute, funded by the State of California to control matter at the nanometer scale and to commercialize discoveries in nanosystems. The workshop brought together 34 leading industrial, academic, and governmental designers of advanced nanoscale probes (both scanning probes and beam tools such as X-ray and electron microscopes), and metrologists who push such probes to their limits to study scientific or technical problems. As intended, the workshop spurred lively discussions about relative merits of techniques, capabilities that are needed, etc., among these disparate leaders in the field, who generally would otherwise not end up talking with each other.