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DNA Functionalization of Carbon Nanotubes for Ultrathin Atomic Layer Deposition of High κ Dielectrics for Nanotube Transistors with 60 mV/Decade Switching

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Single-walled carbon nanotubes (SWNTs) are advanced quasi-1D materials for future high performance electronics.[1−6] SWNT field effect transistors (FETs) outperform state-of-the-art Si FETs owing to near ballistic electrical transport, chemical robustness, lack of surface dangling bonds, and sustained electrical properties when integrated into realistic device structures. One of the goals of transistor down-scaling is to obtain low subthreshold swing S approaching the theoretical limit of 60 mV/decade for device operations at low voltages and power dissipations.

For SWNT FETs, vertical scaling of high κ dielectrics by atomic layer deposition (ALD)[7,8] currently stands at $t_{ox} \approx 8$ nm with $S \approx$ 70−90 mV/decade at room temperature.[1,3] ALD on free-standing SWNTs is incapable of producing a uniform and conformal dielectric layer due to the lack of functional groups on nanotubes[1,9] and because nucleation of an oxide dielectric layer in the ALD process hinges upon covalent chemisorption on reactive groups on surfaces.[7,8] Existing SWNT FETs with high κ dielectrics rely on ALD nucleation and growth on OH terminated SiO_2 substrates and "spill over" to passively cover SWNTs lying on the SiO_2.[1] ALD of relatively thick high κ films (≥8 nm) are needed to fully cover the SWNTs and avoid gate leakage. Recently, Gordon and co-workers covalently modified SWNTs by nitrodiazonium to afford conformal ALD coating (10 nm HfO_2) on the sp^3-modified tubes owing to enhanced nucleation of high κ dielectrics on the nitrogroups on the SWNT sidewalls. Annealing was then used to recover the sp^2 structures of the SWNTs and electrical conductance.[9]

Here, we show that by noncovalent functionalization of SWNTs with poly-T DNA molecules (dT40, Figure 1a), one can impart functional groups of sufficient density and stability for uniform and conformal ALD of high κ dielectrics on SWNTs with thickness down to 2−3 nm (Figure 1b). This enables us approaching the ultimate vertical scaling limit of nanotube FETs and reliably achieving $S \approx 60$ mV/decade at room temperature. We have also carried out microscopy investigations to understand ALD processes on SWNTs with and without DNA functionalization.

Our nanotube FETs were fabricated by patterned growth of SWNTs on 500 nm-SiO_2/Si substrates,[10] lithographic metal (0.5 nm Ti/20 nm Au contacts) source-drain (S−D) formation, functionalization of the exposed length of SWNTs bridging S/D by soaking the device chip in a 10 μM DNA water solution for 30 min followed by 2-min gentle sonication, thorough water rinsing, and drying under N_2. ALD of HfO_2 on the chips at 90 °C using tetrakis(dimethylamido)hafnium $Hf(NMe_2)_4$ and H_2O as precursors[8] and patterning of metal top-gate underlapping[3] the S/D (gate length ≈ 100 nm, Figure 1c) were then carried out (see Supporting Information).

Without DNA functionalization, severe gate leakages and shorts were observed for most of SWNT FETs with high κ thickness $t_{ox} \leq 5$ nm. With DNA functionalization, high performance nanotube−high κ FETs free of gate-leakage currents were reliably obtained with HfO_2 $t_{ox} \approx 3$ nm (Figure 2, diameter of SWNT $d \approx 1.2$ nm). All of our $t_{ox} = 3$ nm DNA functionalized SWNT FETs reproducibly reached theoretical limit of $S \approx 60$ mV/decade at 300 K (Figure 2a) and high transconductance of 5000 S m^{-1} (Figure 2b). For our SWNT FETs with underlapping top-gate, the subthreshold swing S is due to thermally activated on/off switching and $S = \ln(10)\cdot[dV_{gs}/d(\ln I_{ds})] = (k_BT/e)\ln(10)(1 + \alpha)$, where k_B is the Boltzmann constant, and α depends on various capacitances in the device. The fact that we are reaching the theoretical limit of $S = (k_BT/e)\ln(10) \approx 60$ mV/ decade at 300 K suggests $\alpha \approx 0$ and that the gate capacitance is much higher than other capacitances in the device. For 3 nm HfO_2 (Figure 2c), the gate dielectric capacitance per unit length is $C_{OX} \approx 2\pi\epsilon_0\epsilon/\ln(2t_{ox}/R) \approx 6$pF/cm, where $\epsilon \approx 25$ for HfO_2 and R is the radius of the SWNT. This exceeds the quantum capacitance[3] $C_{QM} \approx 4$pF/cm of SWNTs resulted from the finite density of states in the nanotube electronic structure. Thus, with

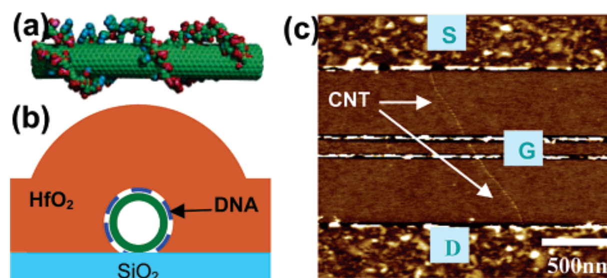

Figure 1. DNA functionalization for nanotube electronics. (a) Schematic of a DNA coated SWNT. (b) Cross-sectional view of HfO_2 (~3 nm by ALD) conformally deposited on a DNA functionalized nanotube lying on a SiO_2 substrate. (c) Atomic force microscopy (AFM) image of a high κ SWNT FET with top-gate (G) underlapping source (S) and drain (D).

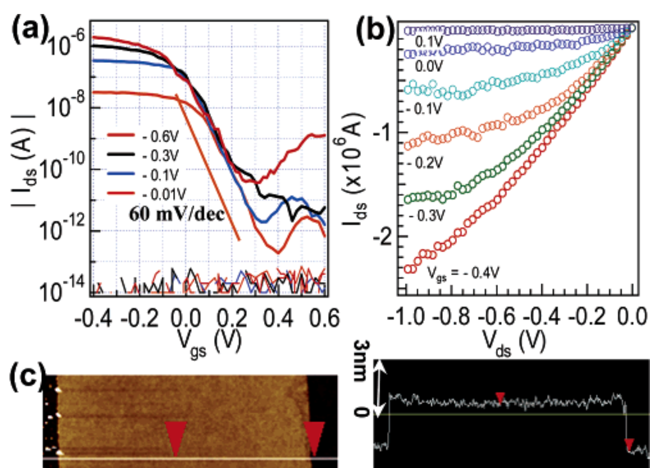

Figure 2. DNA-functionalized SWNT-FET with ~3 nm high κ gate dielectrics. (a) Current vs top-gate voltage (I_{ds}−V_{gs}) curves of the device in Figure 1c recorded at various bias (V_{ds}) indicated. Top-gate leakage currents (bottom traces) under various V_{ds} during V_{gs} sweeps are negligible. (b) Source-drain current-bias (I_{ds}−V_{ds}) characteristics of the device recorded at various top-gate V_{gs} indicated. (c) Thickness measurement of the HfO_2.

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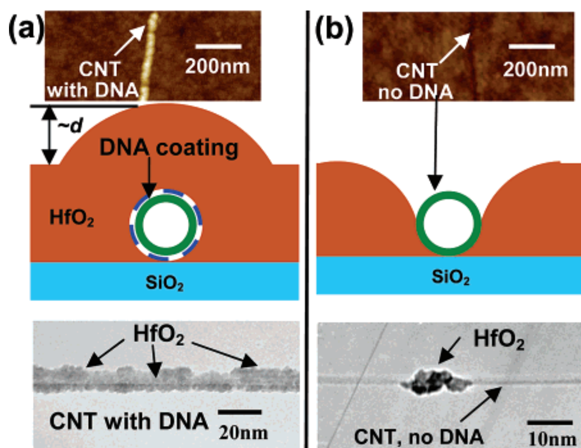

Figure 3. (a) ALD of HfO_2 coatings on SWNTs with and (b) without DNA functionalization, respectively. (Top panel) AFM images of ∼ 5 nm thick HfO_2 coatings on SWNTs lying on SiO_2. (Middle panel) cross-sectional view of the coating profiles. (Bottom panel) TEM images of nominally 5 nm thick ALD-HfO_2 coating on suspended SWNTs.

$t_{ox} = 3$ nm HfO_2 gate dielectrics, we are well into a regime where the total gate capacitance of a SWNT FET is dominant by C_{QM}. Notably, with noncovalent DNA functionalization, we observed no degradation in the SWNT FET conductance after the functionalization and subsequent ALD.

For SWNTs on SiO_2 substrates with DNA functionalization, we observed concurrent ALD of HfO_2 on both nanotube and SiO_2 surfaces, evidenced by the post-ALD topographic height difference (between the nanotube site and the surrounding) being approximately the tube diameter d (Figure 3a top and middle panels). In contrast, for SWNTs on SiO_2 without DNA functionalization, "grooves" were observed along the nanotubes after ALD of HfO_2 (Figure 3b top and middle panels), indicating the lack of nucleation and growth of HfO_2 directly on the tube surface and engulfing of the tube by HfO_2 grown on the SiO_2. We also carried out ALD on suspended SWNTs grown on transmission electron microscopy (TEM) grids. With DNA functionalization, suspended SWNTs allowed for quasi-continuous and conformal HfO_2 coating by ALD (Figure 3a bottom). This differed from "balling up" of high κ material locally on as-grown tubes presumably on defect sites (Figure 3b bottom).[1,9]

Our microscopy data provides direct evidence of enhanced nucleation and growth of HfO_2 on the sidewalls of DNA-functionalized SWNTs in ALD. DNA is known to noncovalently adsorb[11] on SWNT sidewalls via π-stacking[12] of the base-pairs. Such functionalization is found here to be thermally stable at the ALD temperature of 90 °C. We suggest that the functional groups in DNA molecules (including free OH at the 3′-end and oxygen on the phosphate backbone of DNA) are likely involved in chemisorption of precursor species in the ALD process, affording nucleation sites for the deposition of HfO_2 on nanotubes. We have found that functionalization of SWNTs by random-sequence DNA affords less uniform HfO_2 coating on SWNTs than dT40 DNA, likely a result of denser packing on SWNTs and higher ability of solubilizing SWNTs in aqueous solutions of the latter.[11]

We attempted pushing the thickness limit of high κ on DNA-functionalized SWNTs and reached a $t_{ox} \approx 2$ nm lower limit, below which the uniformity of HfO_2 on SWNTs appeared insufficient to avoid gate leakage. For $t_{ox} \approx 2$ nm SWNT FETs (Figure 4), we obtained $S \approx 60$mV/decade and $I_{on}/I_{min} > 10^4$ at $V_{ds} = -0.6$ V (Figure 4a, I_{min} defined as current at the dip of the curve).

Vertical scaling of high κ dielectrics for SWNT FETs below the $t_{ox} \approx 4-5$ nm scale affords no further enhancement in transistor switching once $S \approx 60$ mV/decade and quantum capacitance are reached. Nevertheless, such scaling is useful for investigating

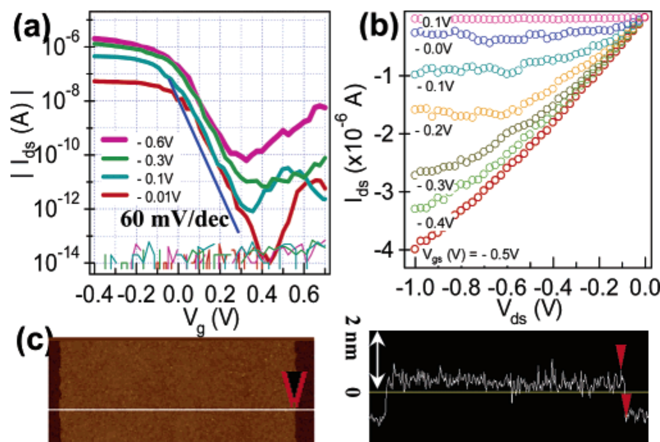

Figure 4. A DNA-functionalized SWNT-FET ($d \approx 1.2$ nm) with ∼2 nm high κ dielectrics. (a,b) Device characteristics. Top-gate leakage currents (bottom traces in a) under various V_{ds} during V_{gs} sweeps are negligible. (c) AFM image (left) and topography (right) of the ∼2 nm thick HfO_2.

interesting device physics in quasi-1D systems such as electron tunneling. In a 1D channel, electrostatics is dependent on the gate dielectric thickness and widths of tunnel barriers (Schottky, band-to-band tunneling BTBT[13] etc.) are often set by t_{ox}.[15] Indeed, for SWNT FETs with similar tube diameters of $d \approx 1.2$ nm, reduction of $t_{ox} \approx 3$ nm (Figure 2) to 2 nm (Figure 4) led to increased ambipolar n-channel currents in the latter. The n-channel currents are due to BTBT, and a thinner high-κ affords sharper band bending at the edges of the top-gate by the gate potential, thus giving rise to a smaller BTBT width and higher tunnel current. It is proposed recently that BTBT may be utilized to obtain tunnel transistors[14] with S beating the 60 mV/decade limit of conventional FETs. The ultrathin high κ described here should be desirable for such devices. Indeed, under $V_{ds} = -0.01$V, we observe $S \approx 50$ mV/decade in the n-channel of our device (Figure 4a red curve), signaling sharp turn-on of BTBT currents resulted from excellent electrostatic gate control. Thus, noncovalent functionalization can be used to enable ultrathin dielectrics for advanced nanotube electronics.

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Supporting Information Available: Experimental details, This material is available free of charge via the Internet at http://pubs.acs.org.

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Supplementary Information

Nanotube growth, DNA functionalization, dielectric deposition and FET device fabrication processes. SWNTs were grown by chemical vapor deposition on SiO_2 /Si substrate from an array of patterned catalyst sites (see ref.10). The substrates were prepared by wet thermal oxidation of heavily doped p-type Si wafers at 1000 ºC to afford 500nm thermal SiO_2. Small diameter semiconducting SWNTs (d<1.5nm, measured by atomic force microscopy) were chosen for device fabrication in the current work. The small diameter tubes have large band-gaps and can afford higher on/off ratios for SWNT FETs. Source(S) and drain(D) electrodes (distance between opposing edges of S/D was 1.5 micron) were fabricated by electron beam lithography (EBL) patterning of PMMA spun on the substrate, development of the EBL exposed S/D regions, 0.5nm Ti/20nm Au deposition by electron beam evaporation, and then liftoff of PMMA in acetone. The chip was annealed in argon at 300ºC for 10min to improve the contacts between the SWNTs and the S/D metal.

For DNA functionalization of the SWNT segments between the S/D electrode pairs, an oligonucleotide consisting of 40 thymine residues (dT40, Stanford PAN Facility) was used. The SWNT device chip was placed and nutated in a 10 μM dT40

DNA water solution for 30min, followed by 2-min gentle sonication of the chip in pure water and then rinsing and drying under a nitrogen stream. ALD of HfO_2 on the chip was carried out at 90ºC using tetrakis(dimethylamido)hafnium(IV), $Hf(N(CH_3)_2)_4$ (Sigma-Aldrich) and H_2O vapor as precursors. For each cycle of ALD, the H_2O vapor pulse was 0.5s in duration, followed by a 360s purging time, a 2s Hf-precursor pulse and then a 120s purging time. The deposition rate under such ALD condition was ~ 0.13nm per cycle. For the 3 nm HfO_2 deposition (Fig. 2), we used ALD 24 cycles and for the 2 nm case (Fig.4) we used 16 cycles. After the ALD step, top-gate (Pt) under-lapping the S/D (100nm gate length) was formed by EBL patterning of PMMA, Pt (18nm) metal evaporation and lift off in acetone.

Measurement of the thickness of high-κ dielectrics deposited by ALD. We always placed a test chip together with the real device chips into the ALD system for dielectric deposition, and the test chip was used for measuring the thickness of HfO_2 deposited. The test chip (SiO_2/Si) contained 5µm by 5µm PMMA windows patterned by EBL (see Fig.1S below). After ALD, we lifted off the PMMA in acetone and carried out AFM imaging of the 5µm by 5µm HfO_2 island (Fig.1S) formed on the test chip SiO_2 substrate. The topographic height of the island corresponded to the thickness of the deposited dielectric film. From such measurements, we found that 24 ALD cycles produced ~ 3nm thick HfO_2 and 16 ALD cycles produced ~ 2nm thick HfO_2.

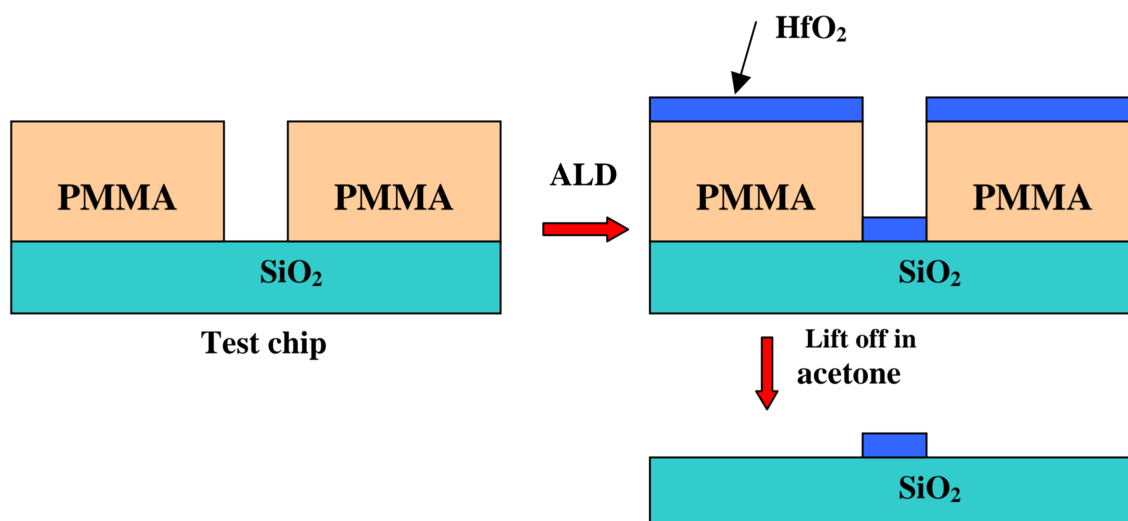

Fig. S1. Schematic illustration of the formation of ALD HfO_2 island for thickness measurement by atomic force microscopy.

Electrical measurements of nanotube FETs.

For all of our electrical measurements, the back-gate (doped Si substrate) was fixed at a constant -20V to turn on the p-channel of the tube-segments outside the top-gate region (see Fig.2S below). Current vs. top-gate voltage (I_{ds}-V_{gs}) curves of the devices were recorded at various bias voltages (V_{ds}) as shown in Fig. 2a and Fig. 4a of the main text. Source-drain current-bias (I_{ds}-V_{ds}) characteristics of the devices recorded at various top-gate V_{gs} (Fig.2b and Fig.4b). The top-gate leakage currents (see bottom traces of Fig.2a in the main text) were always monitored and were well below pA for our 3nm and 2nm high-κ nanotube FETs due to uniform high-κ dielectric coating on the nanotubes.

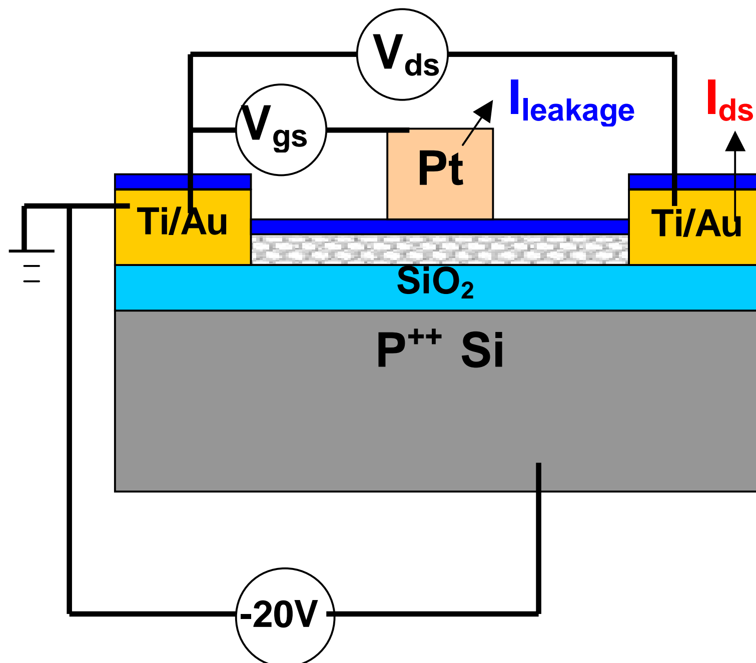

Fig. S2. Schematic experimental setup for nanotube FETs characterization.