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ROBIN Robotics and Intelligent Systems

Adapting Systems by Evolving Hardware

Computer Systems Colloquium (EE380)
Wednesday, 4:15-5:30PM in Gates B01

Stanford EE380, Jan 23, 2008

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University of Oslo, Norway

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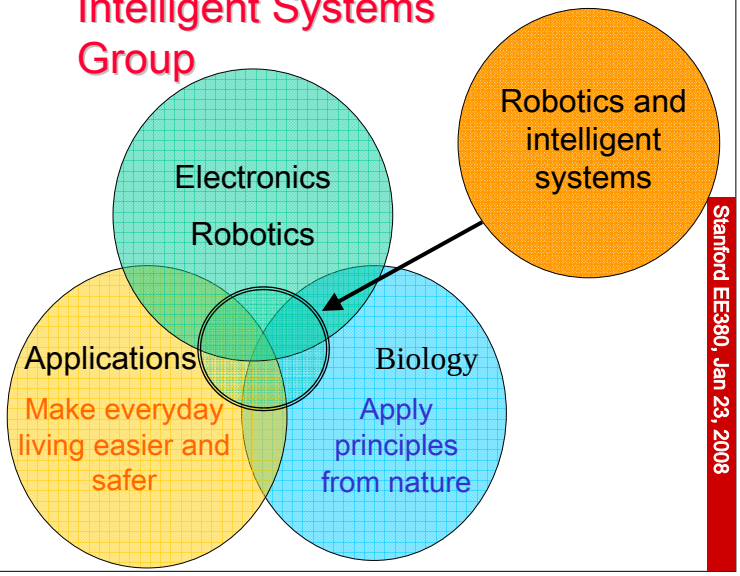
Robotics and Intelligent Systems Group



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Work presented is a collaboration with PhD-student Kyrre Glette

10 COMPUTERWORLD NORGE NYHETER NR. 12 • FREDAG 30. MARS 2007

Endrer adferd med kunstig evolusjon

Ny maskinvare utviklet ved Universitetet i Oslo lærer av ros og endrer adferd gjennom kunstig evolusjon. Målet er et intelligent system som fungerer uavhengig av kommunikasjon med omverdenen.

MORTEN LYSE

Robotikk og Intelligente Systemer

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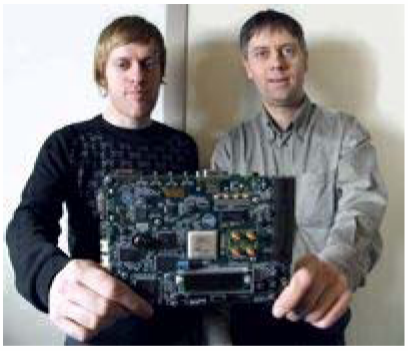

Кирр Глетт (Kyrre Glette) и профессор Джим Торресен (Jim Torresen).

Профессор **Джим Торресен**
Glette) построили развиваю
Hardware - EHW), которые
Иначе говоря, они создали к
эволюционизировать.

Система Торресена и Глетта
аппаратную разработку, кот
чтобы выполнить поставлен
понадобиться 20-30 тысяч ге
система найдет отличную ко
проблемы, и на это может уй

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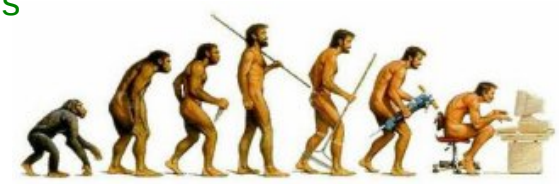
Outline

- Background
- Introduction to evolvable hardware and reconfigurable logic
- Evolving hardware for signal and image classification
- Results
- Conclusions



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Principles of the Nature

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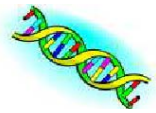
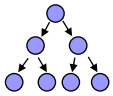
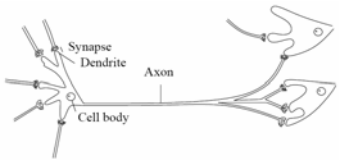
- Evolution: Biological systems develop and change during generations.



- Development: By cell division a multi-cellular organism is developed.



- Learning: Individuals undergo learning through their lifetime.



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Evolution

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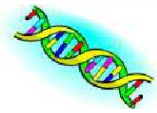

- **Biological evolution:**
  - Lifeforms adapt to a particular environment over successive generations.
  - Combinations of traits that are better adapted tend to increase representation in population.
  - Mechanisms: Selection+Crossover, Mutation and Survival of the fittest.
- **Evolutionary Computing (EC):**
  - Mimic the biological evolution to optimize solutions to a wide variety of complex problems.
  - In every new generation, a new set of solutions is created using bits and pieces of the fittest of the old.
  - Several algorithms are available including Genetic Algorithms (GA) and Genetic Programming (GP)

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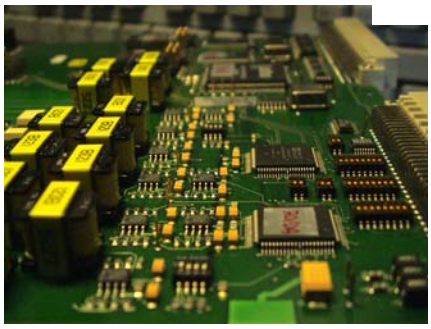
How do we evolve a circuit?

Input/Output Specification → Genetic Algorithm →



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Possibilities of Evolvable Hardware (EHW)

- Two main directions:
  - Tuning/optimizing parameters of a circuit or system (also called evolutionary circuit design).
  - Evolving a system from scratch.
- New features provided:
  - Run-time adaptive hardware
  - Self repairing hardware
- Goal:
  - Make better computing systems than traditional architectures for real-world applications.

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EHW Applied to Real-World Applications

- Analog
  - Adaptive Equalizer
  - Amplifier and Filter Design
  - Analog Circuit Synthesis
- Parameter tuning
  - Clock Timing Adjustment
  - Analog Filter Tuning
- Robot Control
- Image processing
  - Image Compression
  - Image Filtering
  - Image Recognition
- Classification/Recognition
  - Sonar Classification
  - Gene Finding
  - Prosthetic Hand

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Evolving a Circuit

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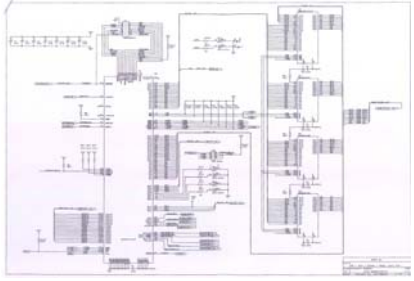
- Define the basic building blocks:
  - Digital (gates or higher level functions)
  - Analog (transistor/resistor/L/C)
- Represent each building block in the chromosome by its **function** and its **connections** to other building blocks in the circuit.



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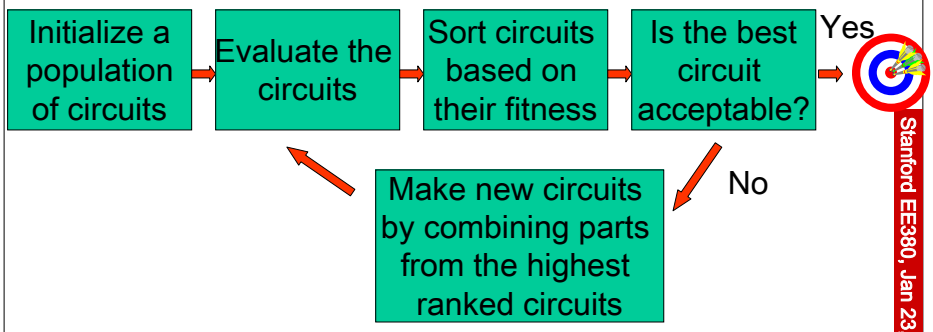
Evolving a Circuit



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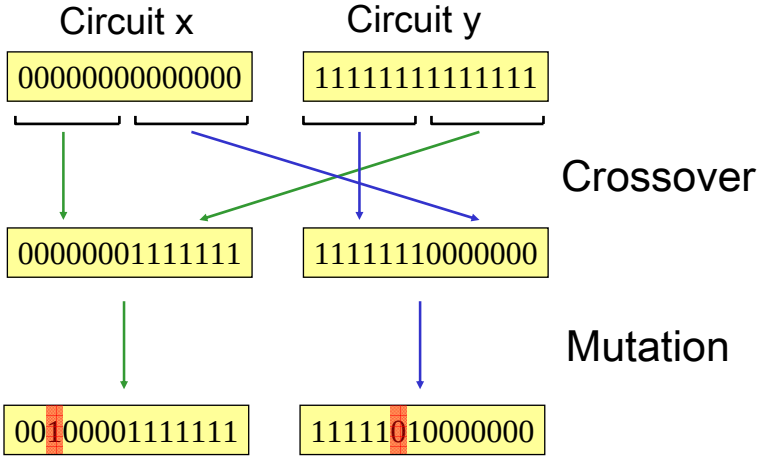
Evolutionary Operators: Genetic Algorithms (GA)



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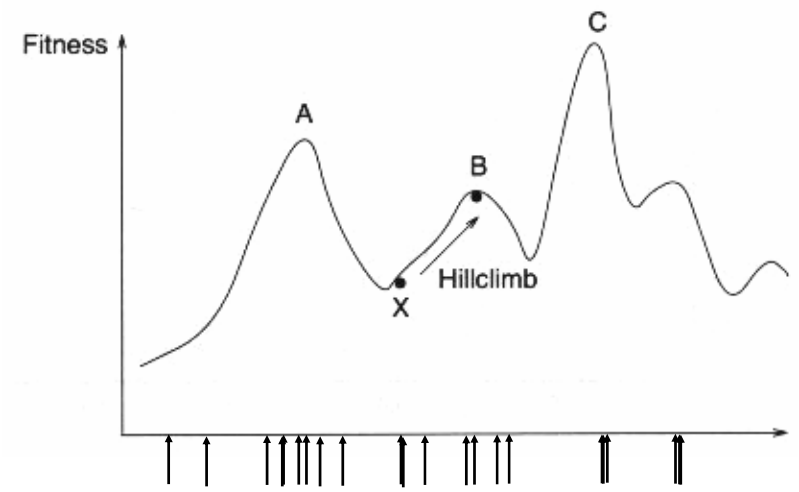
Hillclimbing Problem in Search



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Fitness

- A measure of how well adapted an individual is.
- The value determines the probability of being selected for reproduction.
- The way the fitness function is constructed is critical for the GA performance.

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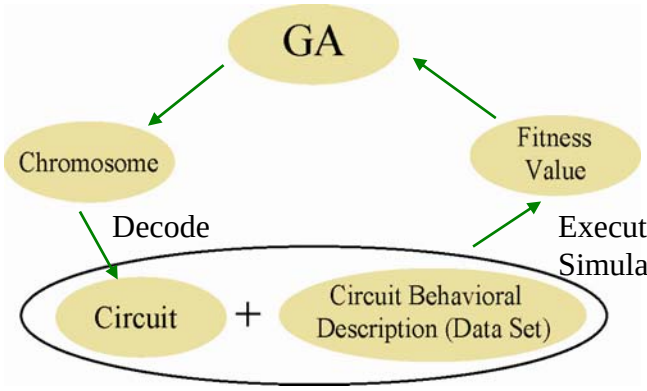
Computing Circuit Fitness



Fitness= $\sum_{p} \sum_{o}$ (match of output o for pattern p)

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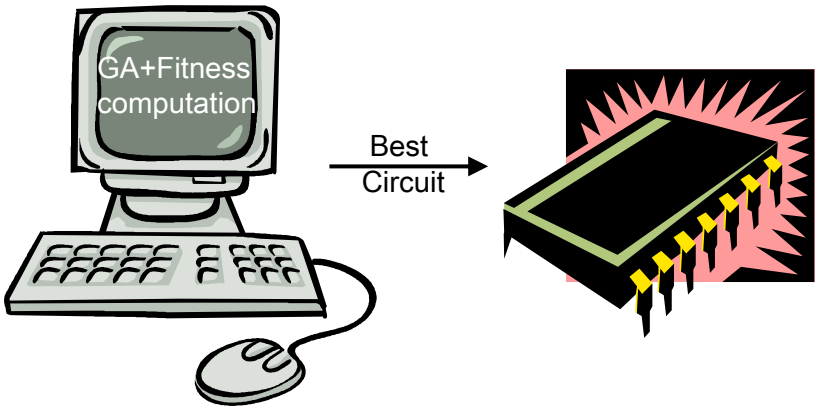
Fitness Computation OFFLINE (extrinsic)



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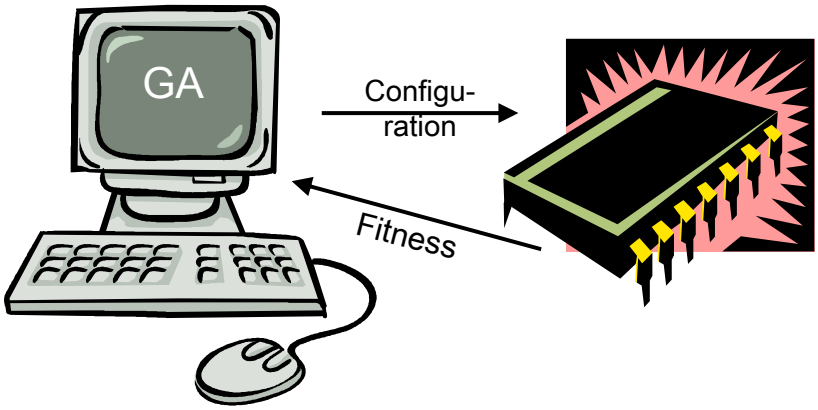
Fitness Computation ONLINE (intrinsic)



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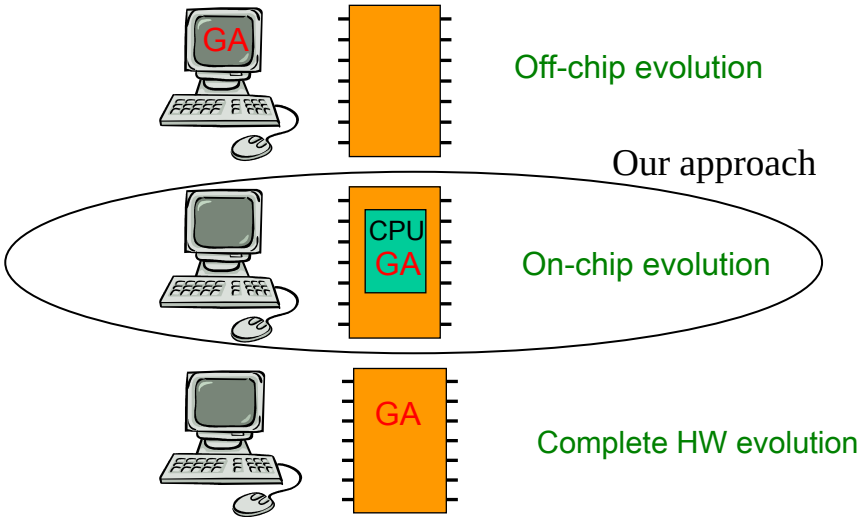
Evolution



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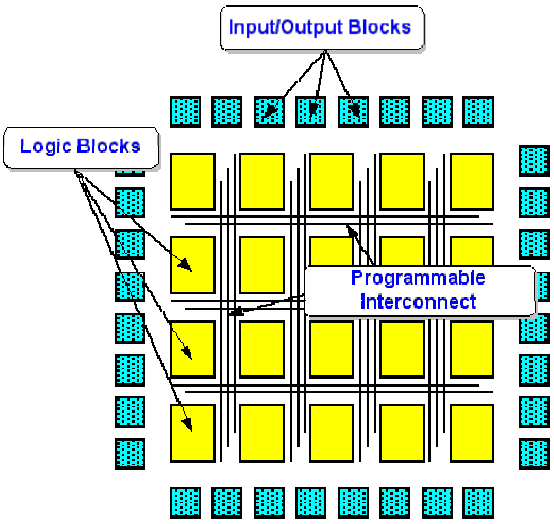
FPGA (Field Programmable Gate Array)



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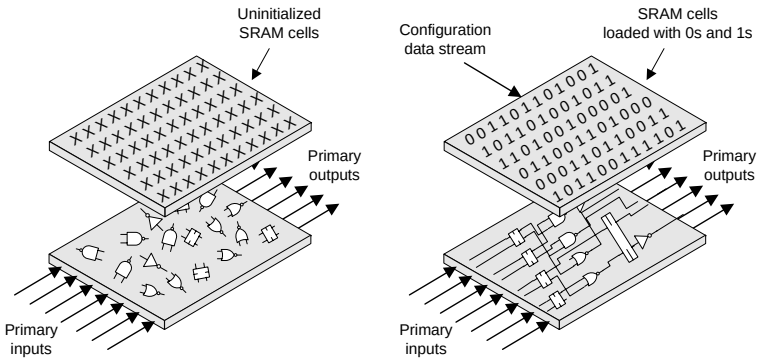
Configuration of FPGA (Field Programmable Gate Array)



(a) Unconfigured (b) Configured

The Design Warrior's Guide to FPGAsDevices, Tools, and Flows.
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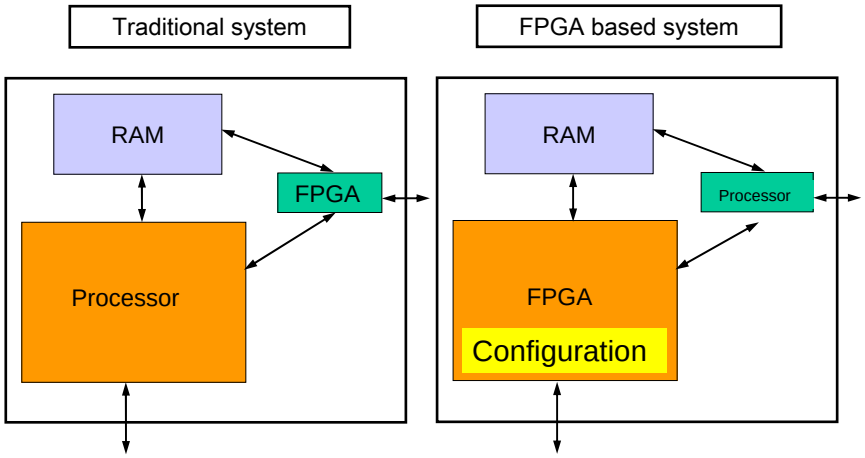
FPGA for Data Processing



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Performance Comparison (Nallatech)

	Microprocessor (P4)	FPGA (2VP100)
Clock speed	3.8 GHz	180 MHz
Internal Memory Bandwidth	122 GBytes per Sec	7.5 TBytes per Sec
# Floating Point Units	2	146
Power Consumption	> 100W	< 10W
Peak Performance	7.6 GFLOPS	26 GFLOPS
Sustained Performance	0.76 GFLOPS	13 GFLOPS
I/O / External Memory Bandwidth	8.5 GBytes/sec	67 GBytes/sec

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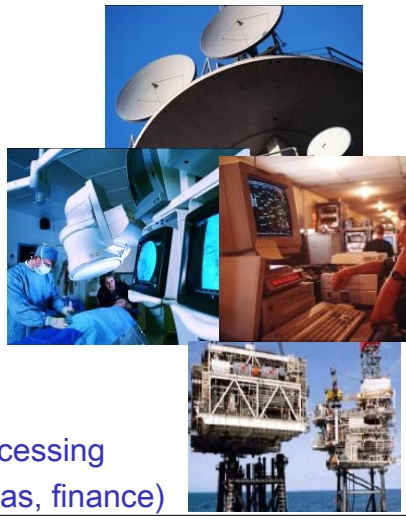
Functions Well Suited to FPGA Acceleration

- Searching
- Sorting
- Signal processing
- Audio/video/image manipulation
- Encryption
- Error correction
- Coding/decoding
- Network packet processing
- Data analysis (oil, gas, finance)



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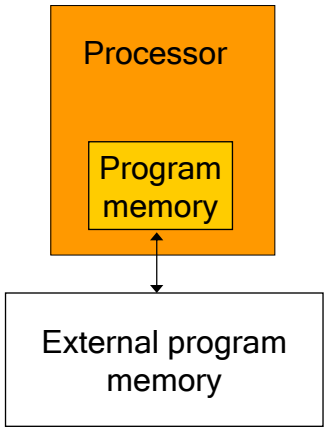
Processor versus FPGA



- SRAM program memory
- Program loaded at startup
- Complete program in internal or external memory
- No swapping to other programs
- Processor technology ~1985
- FPGA technology 2008!

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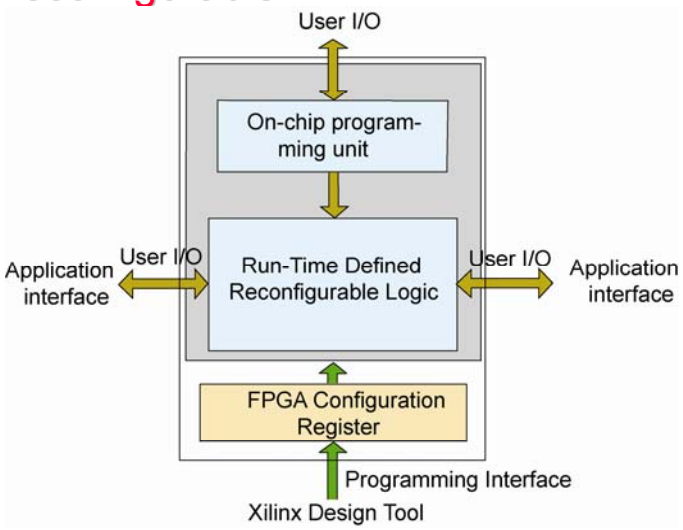
Virtual Reconfigurable Circuit



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System-On-Chip Evolution on Field Programmable Gate Array (FPGA)

- Xilinx Virtex-II Pro FPGA
- A hard (PowerPC) or soft (MicroBlaze) processor core is used
- The processor core runs the evolutionary algorithm
- Evaluation of individuals is performed on the EHW module in the same chip

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Prototyping Board: XUP Virtex-II Pro

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- XC2VP30 Virtex-II Pro FPGA
  - 13969 Slices, 2448 Kb BRAM
  - 2 PPC405 cores
- DDR SDRAM slot
- CompactFlash slot
- VGA, AC97, PS2, RS232, ...

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System-On-Chip

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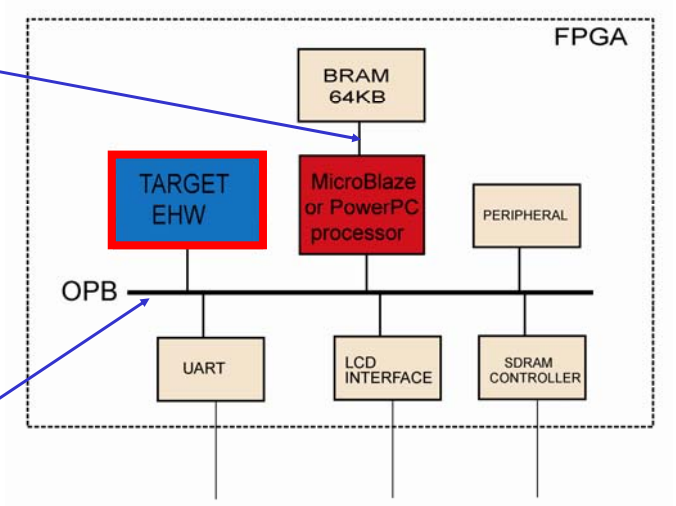
Local Memory Bus – Fast access to program memory

On-chip Peripheral Bus – Used to connect the peripherals in the system



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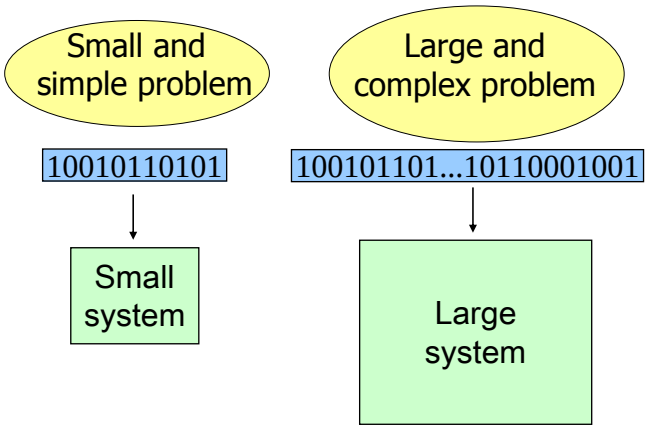
Evolving Systems

Chromosome string representation



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Dividing the application

- **Idea:** Evolve a system gradually (divide-and-conquer the application).
- Partitioned training vectors
- Partitioned training set

Inputs			Outputs		
x_3	x_2	x_1	y_3	y_2	y_1
0	0	0	0	0	1
0	0	1	1	1	0
0	1	0	1	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	1	0	1	0

- **Benefits:**
  - Simpler and smaller search space for the evolution.

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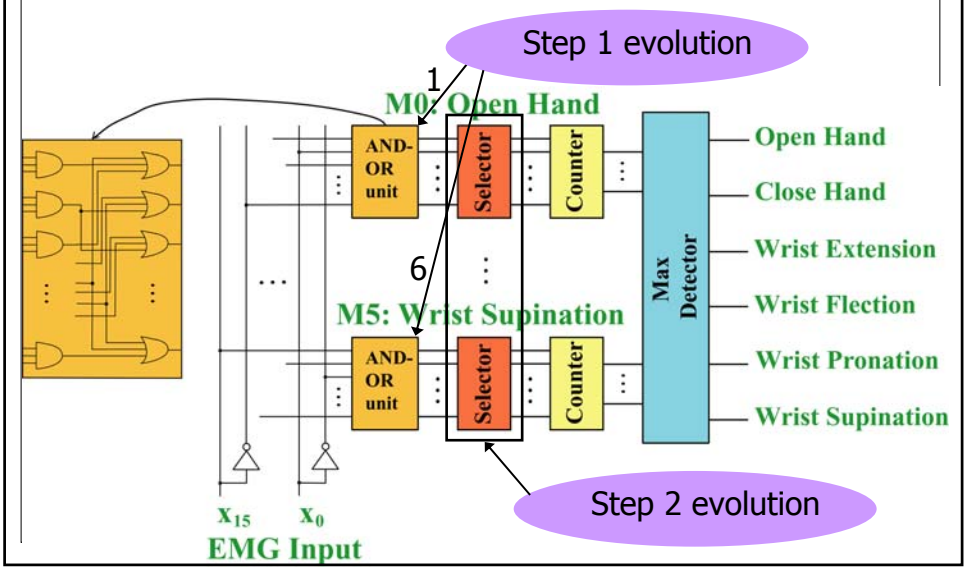
Earlier Architecture: Prosthetic Hand



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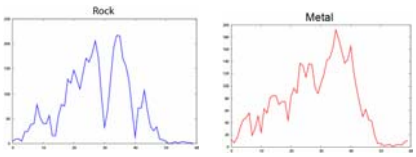
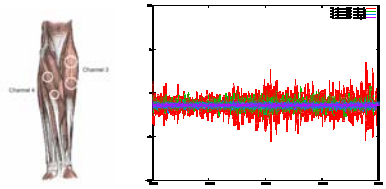
Classification Applications

- Face Image Recognition

- Sonar Return Classification



- Prosthetic Hand Sensor Signal Classification



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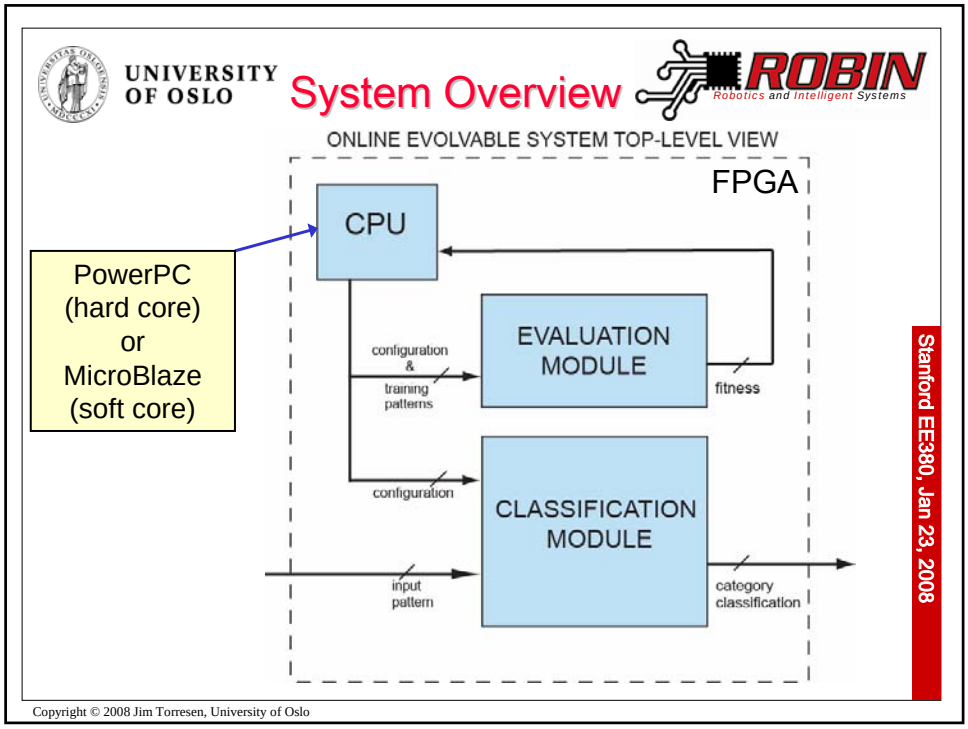
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System Overview
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ONLINE EVOLVABLE SYSTEM TOP-LEVEL VIEW
FPGA
CPU
PowerPC (hard core) or MicroBlaze (soft core)
configuration & training patterns
EVALUATION MODULE
fitness
configuration
CLASSIFICATION MODULE
input pattern
category classification
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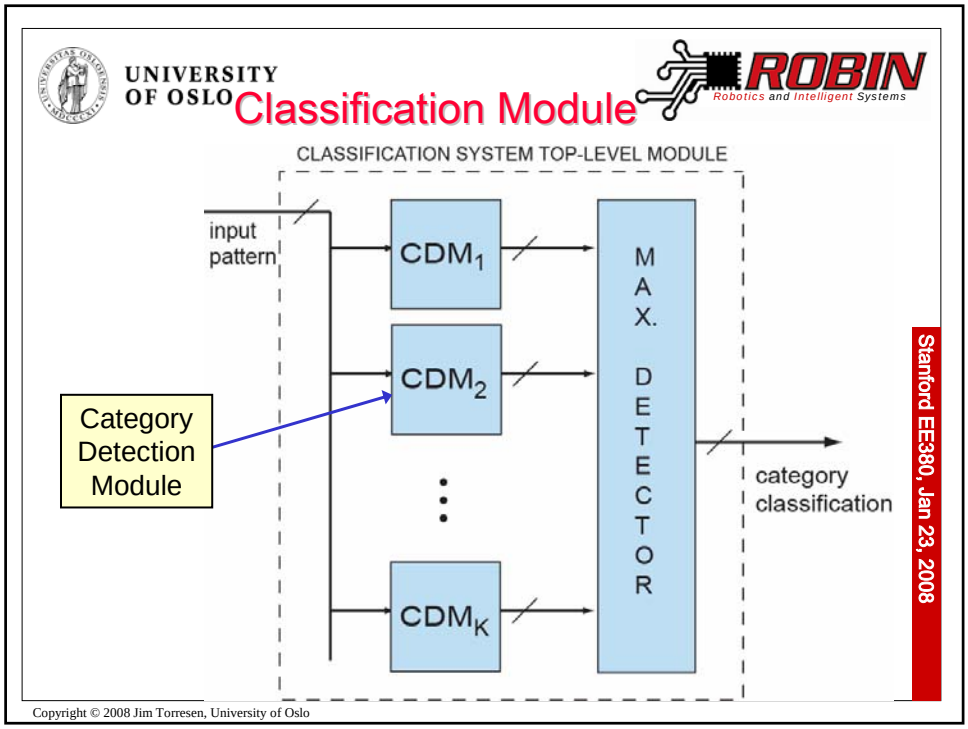
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Classification Module
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CLASSIFICATION SYSTEM TOP-LEVEL MODULE
input pattern
CDM1
CDM2
CDMK
MAX. DETECTOR
category classification
Category Detection Module
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CDM

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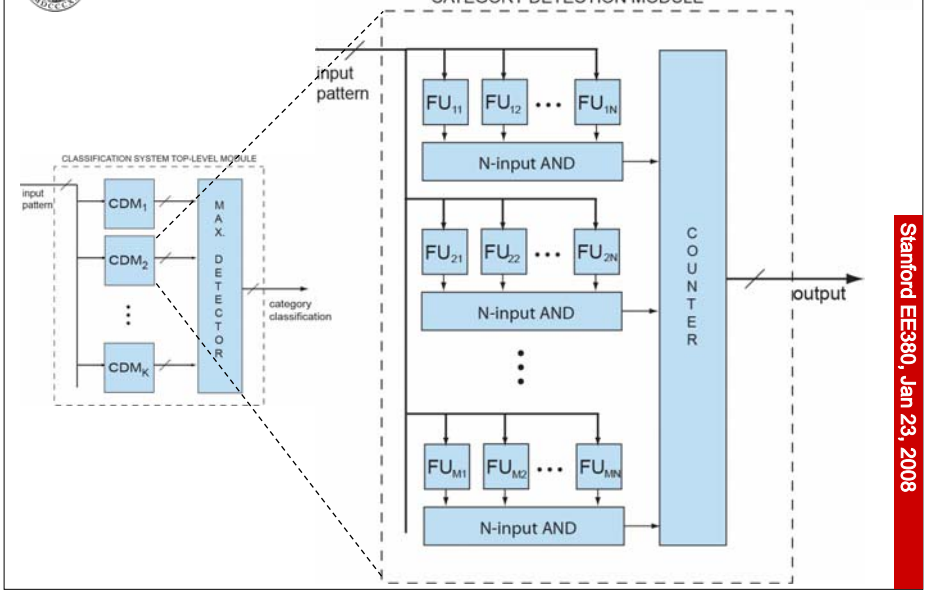

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Functional Unit

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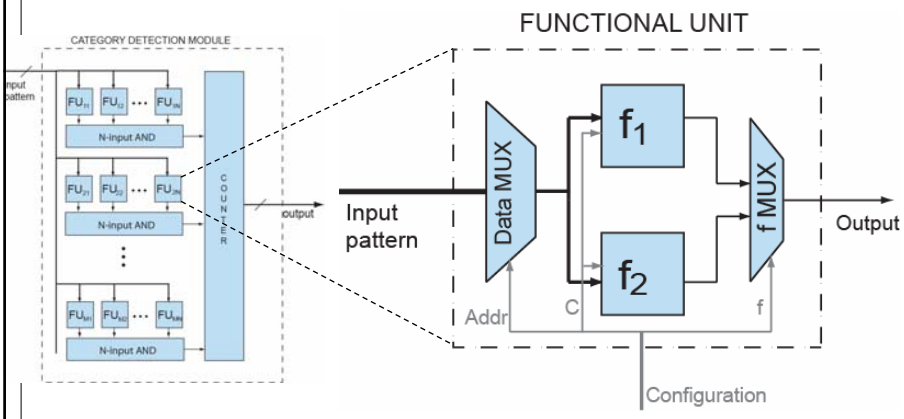

f	Description	Function
0	Greater than	O = 1 if I > C, else 0
1	Less than or equal	O = 1 if I ≤ C, else 0

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Application to be presented

- AT&T Database of Faces (formerly The ORL Database of faces)
  - Classify images of 40 different persons
  - 10 different images of each face

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Input Reduction

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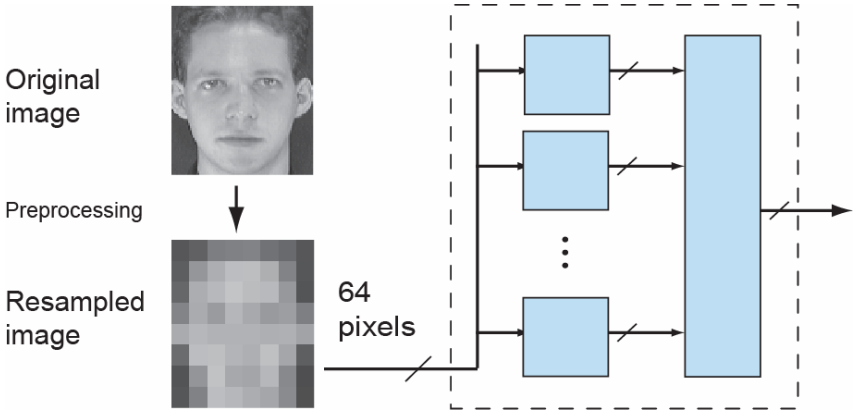

- 92x112 8-bit pixels resampled to 8x8 8-bit pixels
- Input pattern: 512 bits

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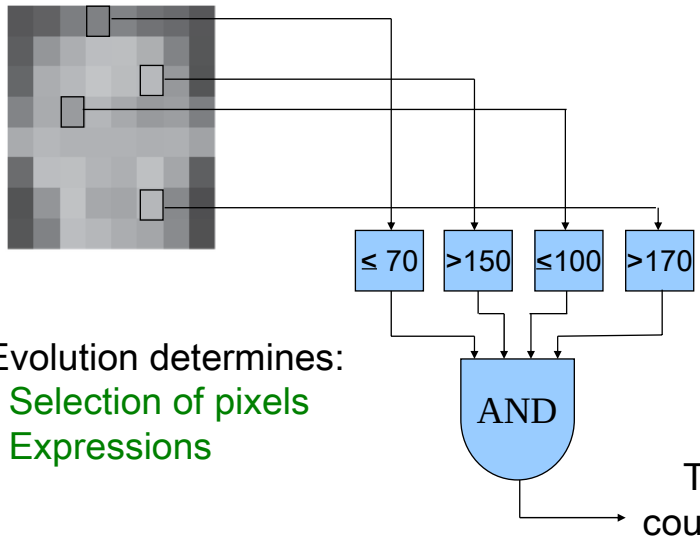
Example: One FU Row



Evolution determines:
- Selection of pixels
- Expressions

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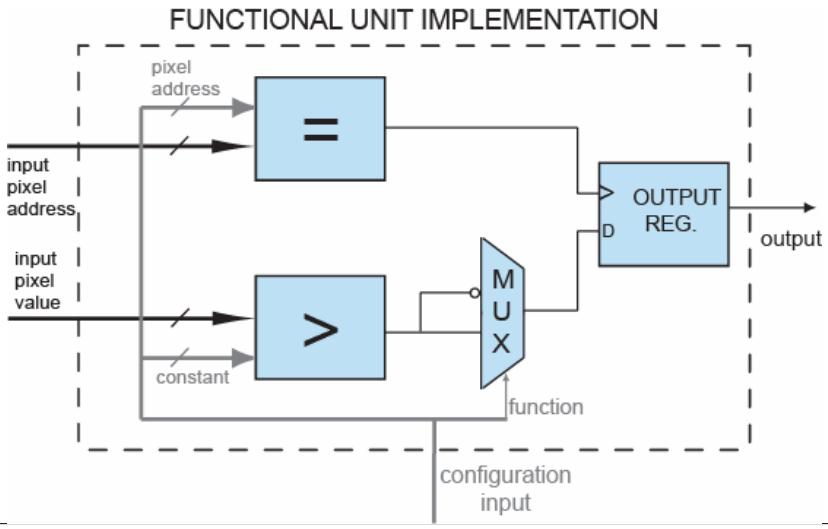
FU HW Implementation



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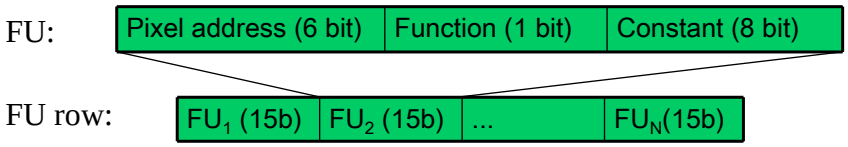
Evolution and Fitness Function



- One FU row can be evolved at a time
- Fitness function emphasizes positive matches of the category being evolved at the moment.

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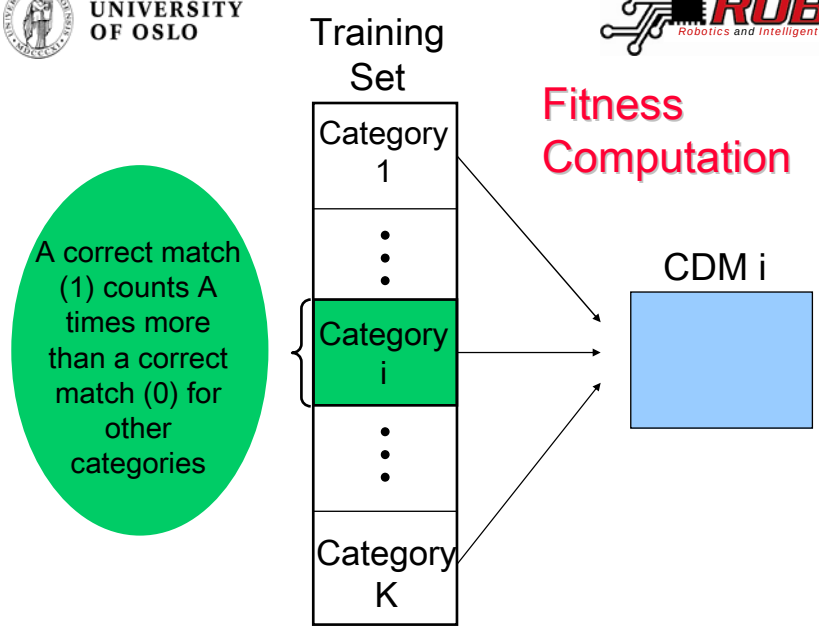
Fitness Computation



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FEM

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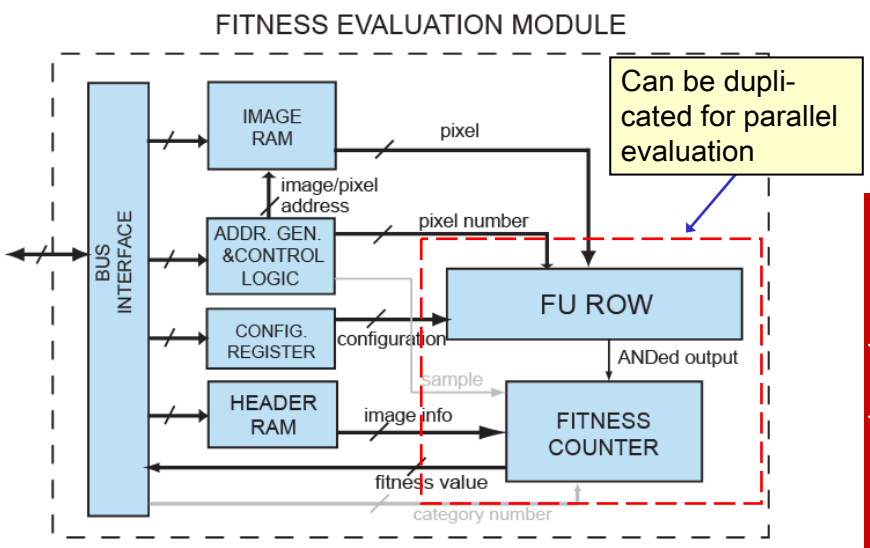

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CDM

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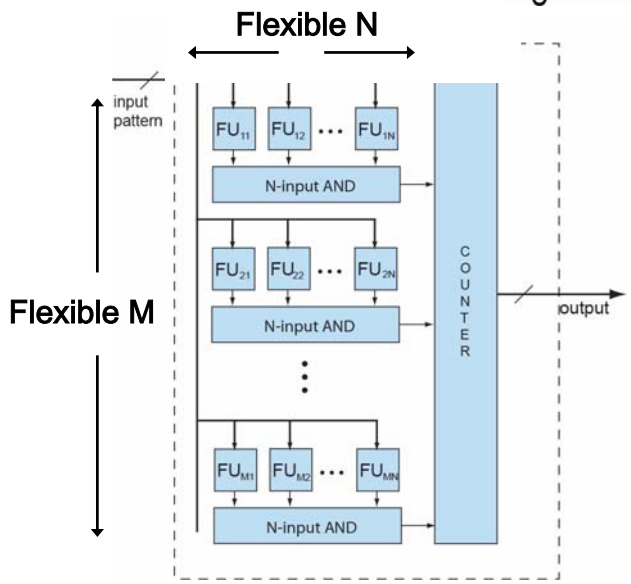

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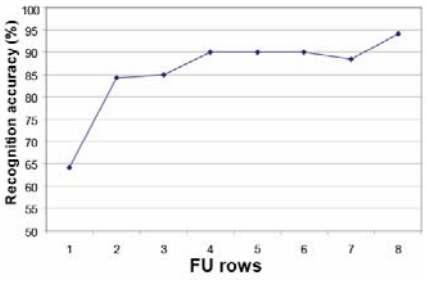
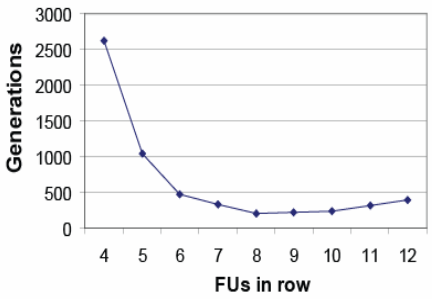
Results: Architecture Parameters





- More FU rows within a CDM gives a higher chance of correct classification
  - Each FU row evolved with random initial values – gives different "rules"
  - The more FU rows in a CDM, the higher the output resolution
- Too few or too many FUs in a row make it more difficult to evolve a classifier

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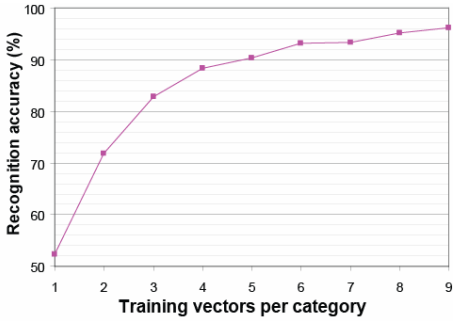
Results: Classification Accuracy



- Using 6 FUs per row and 10 rows per CDM
- Using x training vectors per category and the rest (10-x) as test vectors
- 96.25% accuracy using 9 training vectors per category
  - Better than previous offline EHW architecture
  - Competitive to Eigenfaces or Fisherfaces, SVM (Support Vector Machine) performs better

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HW Implementation

- Implemented on a Xilinx Virtex-II Pro XC2VP30
- Evaluation module: 371 slices (2%)
- Parallel evaluation (8 individuals): 1393 slices (10%)

- Estimated < 1 μs classification time per pattern (@100 MHz), using time multiplexing

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Evolution Speed

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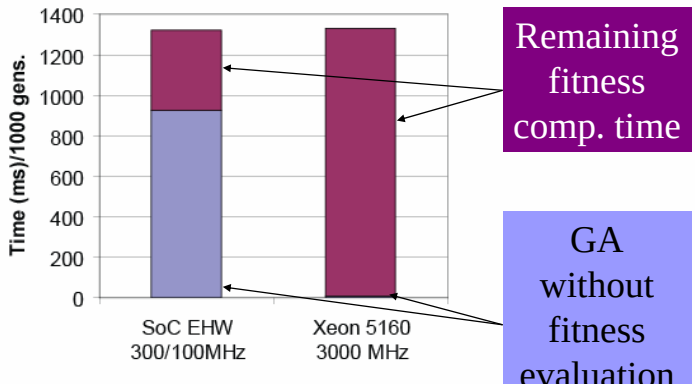

- 8 parallel evaluations
- Fitness evaluation alone is 2.12 times faster in HW
- GA is not fully optimized for the PowerPC

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Input (Sonar)

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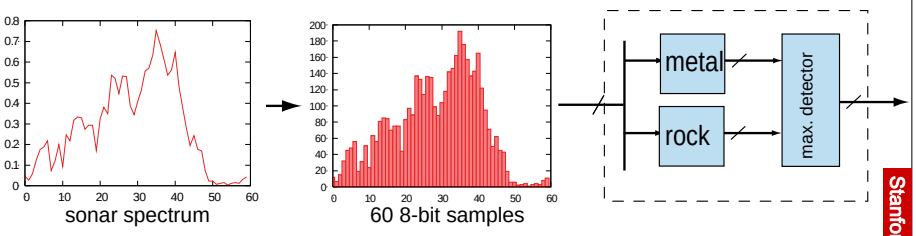

- Original data in float values, converted to 8 bit integers
- 60 samples, 8 bits per sample => 480 bits per input pattern
- Each pattern is presented to all FUs

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Classification Accuracy (Sonar)

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FU rows (M)	Training set (avg.)	Test set (avg.)
20	97.3%	87.8%
58	99.6%	91.4%

- Using 6 FUs per row, average over 10 runs
- 104 training vectors, 104 test vectors (total)

- Better than previous offline EHW architecture
- Better than the original ANN implementation (90.4% avg.)
- SVM performs better (95.2%)

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HW Implementation (Sonar)

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- Implemented on a Xilinx Virtex-II Pro XC2VP30 (XUP2VP)
- Classification module:

FU rows	Slices	% of FPGA
20	3866	28
58	11189	81

- 0.5 μs classification time per pattern (@118 MHz), using time multiplexing
- Evaluation module: 371 slices (2%)
  - Parallel evaluation (8 individuals): 1393 slices (10%)

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System Overview

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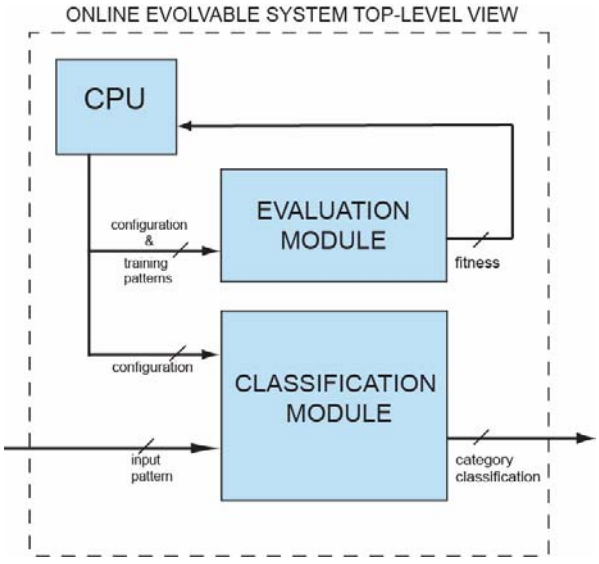

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Evolution Speed (Sonar)

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- Average number of generations required per row is 853 (limit 1000)
- 98948 generations for entire system

- 0.54s per row
- 63s for entire system
  - System is operational after 4.3s (8 rows)

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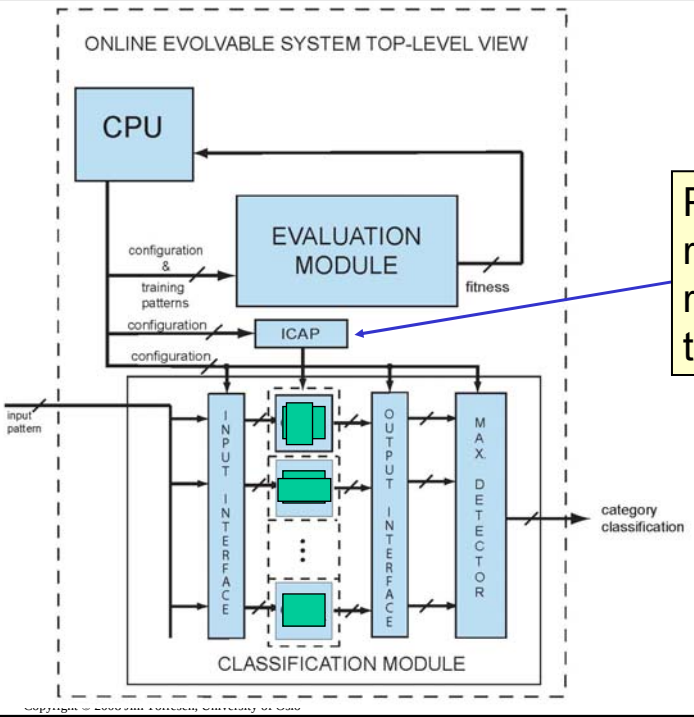

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Partial reconfigu-ration of the CDMs

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Conclusions 1

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- High classification speed
  - Suitable for problems requiring high throughput
- High classification accuracy
  - Comparable or better than other methods (with exception for SVM)
- Incremental evolution
  - Makes evolution of a large system possible
  - Evolution time is short
  - The evaluation module requires few FPGA resources

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Conclusions 2

ROBIN Robotics and Intelligent Systems

- Run-time reconfigurable architecture
  - Allows for online evolution in an on-chip system
  - Suitable for adaptation to a changing fitness function/training set
- Combination of SW/HW on-chip gives benefits
  - Evolution time can be kept down with HW fitness evaluation
  - The rest of the GA can run in SW, allowing for easy modifications
  - A compact system (SoC)

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EHW Conferences

- *International Conference on Evolvable Systems* (ICES). Springer LNCS.
  - Next conference: Prague, Czech Republic
  - Paper deadline: March 19, 2008

- *NASA/ESA Conference on Adaptive Hardware and Systems* (AHS), IEEE.
  - Next conference: Noordwijk, The Netherlands
  - Paper deadline: January 31, 2008

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The Research Council of Norway

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Thank you!

- Please feel free to contact me after this talk.
- Several PhD positions will be available soon (one in our group).
- I'm also available for discussions here at Stanford, Friday January 25.

E-mail: jimtoer@ifi.uio.no
http://www.ifi.uio.no/~jimtoer

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