800Mbaud PHY for 10GBase-T

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Scott Powell, Broadcom
Tetsuya Higuchi, ERI
Albert Vareljian, KeyEye
Jim Wieser, National Semiconductor
Katsutoshi Seki, NEC Electronics
George Zimmerman, Solarflare
Jose Tellado, Teranetics
Toshihiko Shimizu, Tokyo Electric Power Co
Nick Van Bavel, Vitesse

Overview

- Main parameters of PHY proposal
  - LDPC-1K
  - THP-Select
  - Framing and control
  - PAM12-T
- Performance
  - Margin and Noise Immunity
  - EMI
- Proposal Summary

Main parameters of PHY proposal

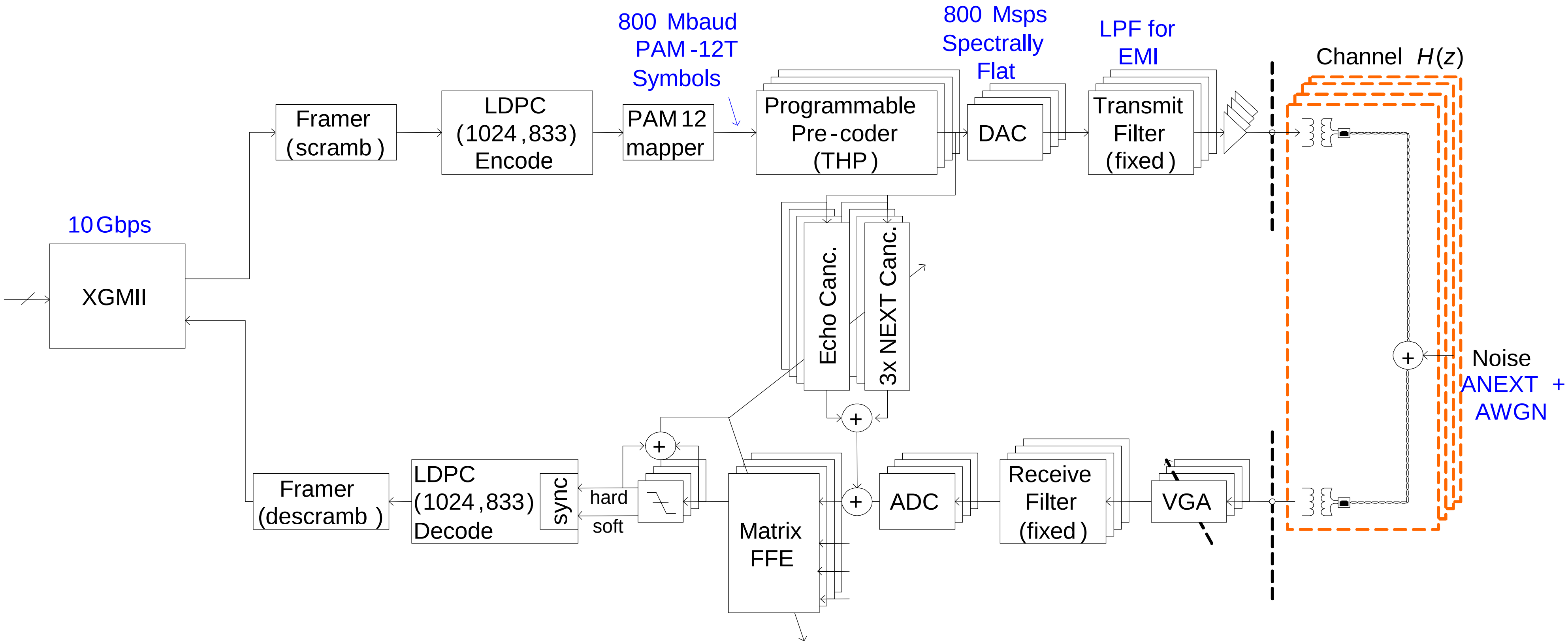
Framing and control:	64B/65B with PAM2 sync headers
FEC code:	LDPC(1024,833), systematic
Modulation code:	Baseband PAM12-Ternary
Equalization:	Start-up Selectable Tomlinson-Harashima precoder at Tx
Symbol rate:	800MHz
Transmit Filter:	Spectral Mask (TBD)
Transmit Power:	5 dBm at MDI

Benefits of PAM12 at 800MHz

- **Theoretical:** PAM12 at 800MHz is very close to the optimum constellation/symbol rate combination, as confirmed by multiple presentations:
    - mcclellan_1_0504.pdf (Solarflare): Optimum is 770MHz (model1 in slide 5)
    - takatori_1_0504.pdf (KeyEye): Optimum is 833MHz (model 1, 2, 3 in slides 4, 5, 6)
    - tellado_1_0704.pdf (NEC Elect, Teranetics): Optimum is 800MHz (model 3, slide 32)
    - ungerboeck_1_0504.pdf (Broadcom): Optimum is 800MHz (model 3, slides 15, 16)

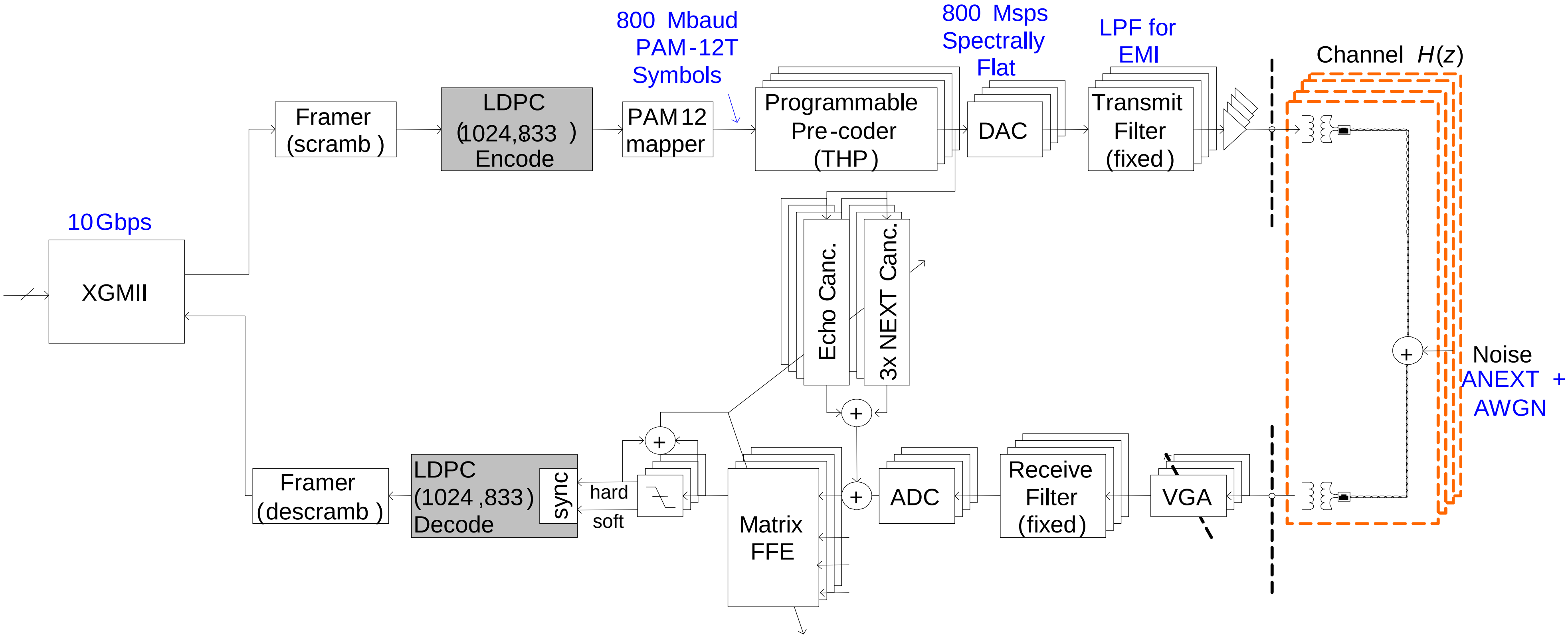
- **Implementation:**
  - PAM12T symbol rate ~20% lower than PAM8
    - Echo, NEXT, FEXT cancellers and equalizers are ~20% shorter
    - Digital and Analog clocks operate ~20% slower
    - Shorter cancellers and slower clock result in 20-40% reduction in digital power consumption relative to PAM8
  - PAM12T bandwidth is ~20% less than PAM8, leading to simpler filters, transformers, connectors, etc.
  - PAM12T latency is half that of PAM8

Example System Architecture



- **Implementation used for analysis**
- **Other implementations possible**

LDPC

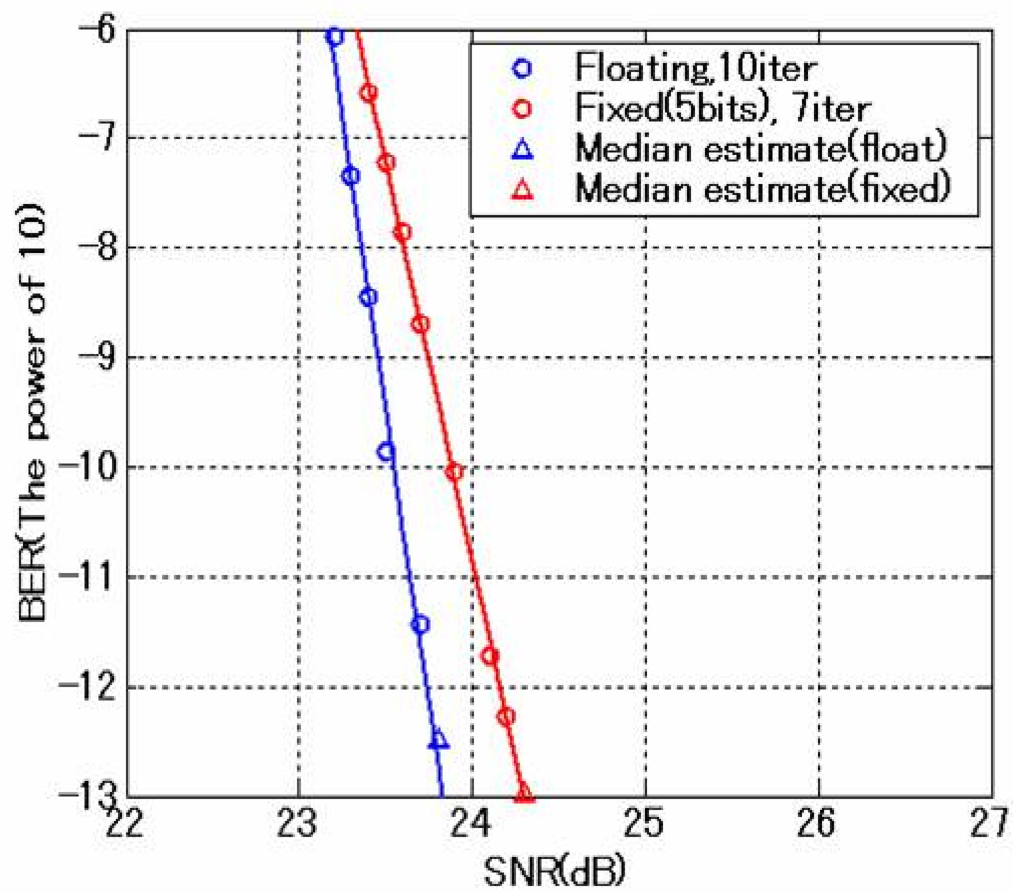


800 Mbaud
PAM-12T
Symbols
800 Msps
Spectrally
Flat
LPF for
EMI
Channel $H(z)$
10Gbps
XGMII
Framer
(scramb)
LDPC
(1024,833)
Encode
PAM12
mapper
Programmable
Pre-coder
(THP)
DAC
Transmit
Filter
(fixed)
Echo Canc.
3x NEXT Canc.
Noise
ANEXT +
AWGN
Framer
(descramb)
LDPC
(1024,833)
Decode
sync
hard
soft
Matrix
FFE
ADC
Receive
Filter
(fixed)
VGA

LDPC(1024,833) PAM12 Performance

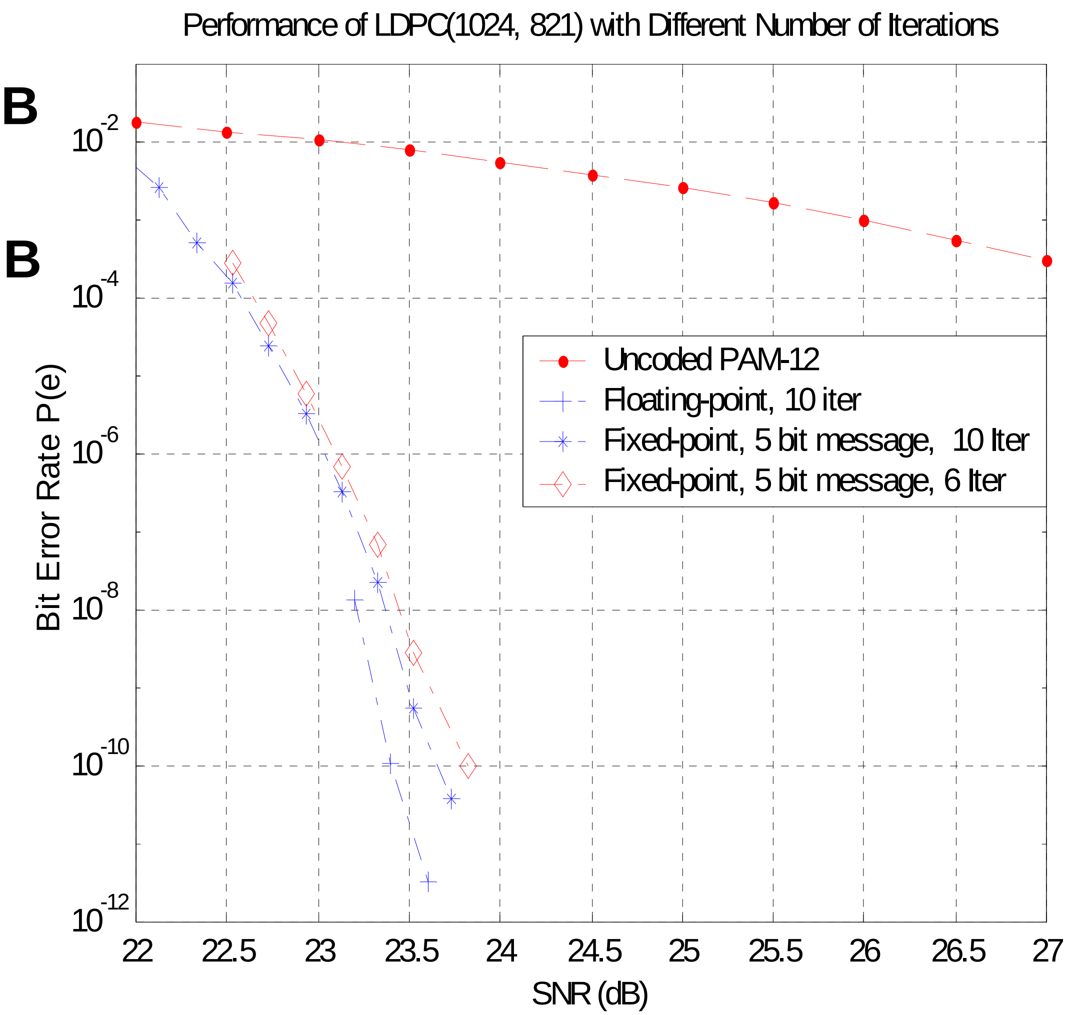
- *SNR for BER < 1E-12:* **23.8 dB**
- *Bits/Symbol:* **3.21**
- *Coding gain:* **10 dB**
- *Avg bit errs/error block:* **25.0**
- *Floating point:* No errors seen in 4E13 bits at SNR= 23.8 dB
- *Fixed point:* No errors seen in 1.4E14 bits at SNR= 24.3 dB
- <u>*No BER slope degradation up to BER = 1E-13*</u>

Error Free SNR points	80% confidence	95% confidence
23.8 Float Point	0.9e-12	1.8e-12
24.3 Fixed Point	0.3e-12	0.5e-12



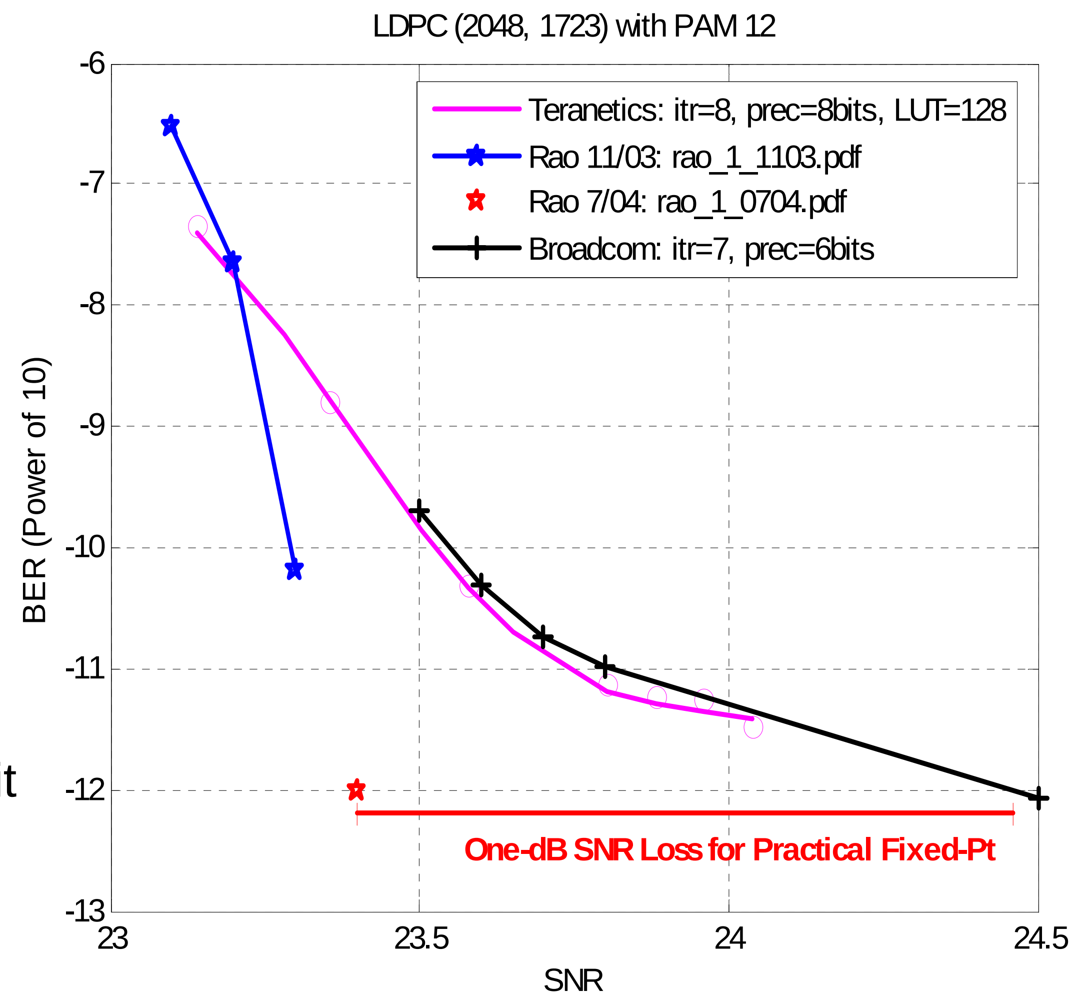
LDPC(1024,821) PAM12 Performance

- *SNR for BER = 1E-12:* **23.7 dB**
- *Bits/Symbol:* **3.18**
- *Coding gain:* **10.1 dB**
- No error floor observed up to BER= 3E-12



LDPC(2048,1723) PAM12 Performance

- Significant BER slope degradation observed below 1E-11 for practical implementations of LDPC SPA decoder
  - Slope change occurs at theoretically predicted point
- Broadcom results use 7 iterations with 6 bit LUT (64 entries)
- Teranetics results use 8 iterations with 7 bit LUT (128 entries)
- Rao's results use 12 iterations with 12 bit LUT (4096 entries).
- A typical LDPC decoder will have 100s or 1000s of LUTs
  - Rao's LUTs are > 40x larger.
- Typical FEC decoders require 3-5 bit fixed point math



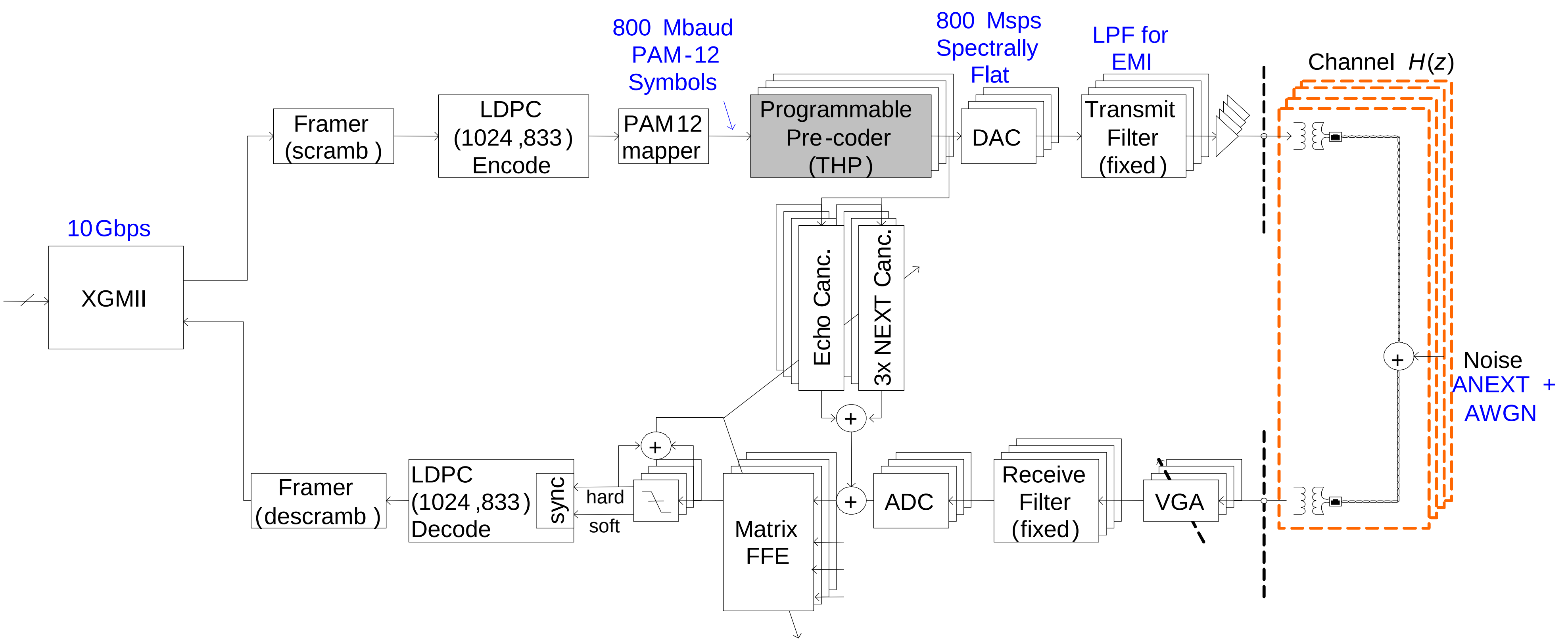
LDPC (1024,833) is best option

LDPC(1024,833) has more robust performance than LDPC(2048,1723) with half the latency.

Code	LDPC(1024,833) PAM12T mapping	LDPC(1024,821) PAM12T mapping	LDPC(2048,1723) PAM12T mapping
Information bits/Symbol	3.21bits	3.19bits	3.27bits
Required SNR for BER=1E-12	23.8 dB Floating Pt 24.1 dB 5bit Fixed Pt	23.7 dB Floating Pt (estimate)	23.4 dB (*1) 24.5 dB 6-7bit Fixed Pt
BER robustness (BER slope)	0.15 dB/BERdecade		0.6 dB/BERdecade
Complexity: Number edges LUT size	10240 32	12288 32	12280 64-128
Shannon bound	19.3 dB	19.2 dB	19.6 dB
Gap to capacity @ BER =1E-12	4.8 dB (fixed pt)		4.9 dB (fixed pt)
Intrinsic Latency Practical Latency (x2.5)	160nsec 400nsec	160nsec 400nsec	320nsec 800nsec
Practical Symbol rate	800MHz	800MHz	781.25MHz
Lower Bound Hamming Distance	12	14	8

*1 : Estimated based on Rao's proposal and re-mapping the code from PAM8 to PAM12

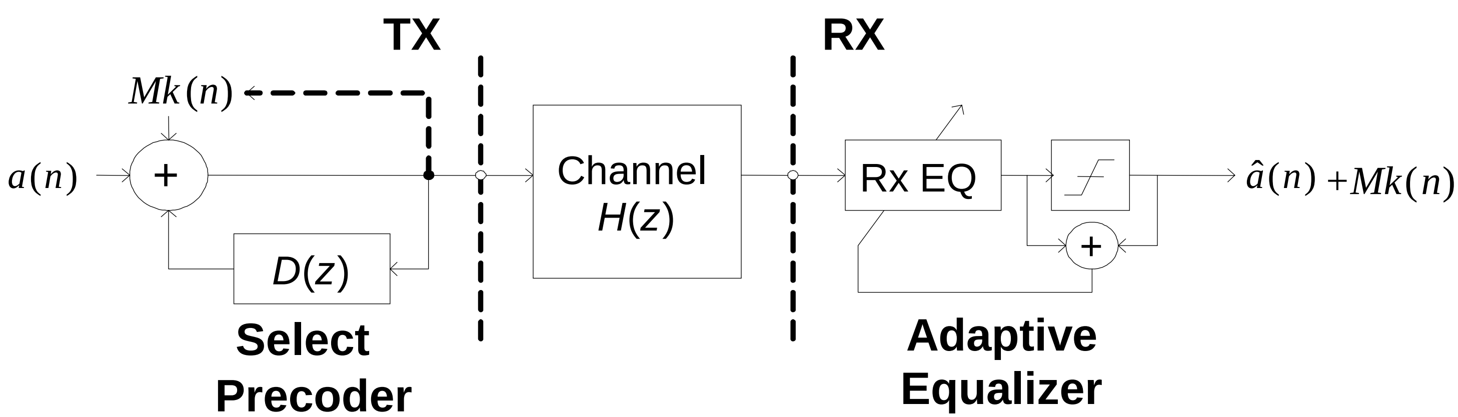
Tomlinson-Harashima Precoding



THP Details

Ref: powell_1_0304.pdf, ungerboeck_1_0704.pdf

- Precoder coefficients *D(z)* selected at autonegotiation/ start-up to approximately match channel response
  - Selected THP is fixed after start-up



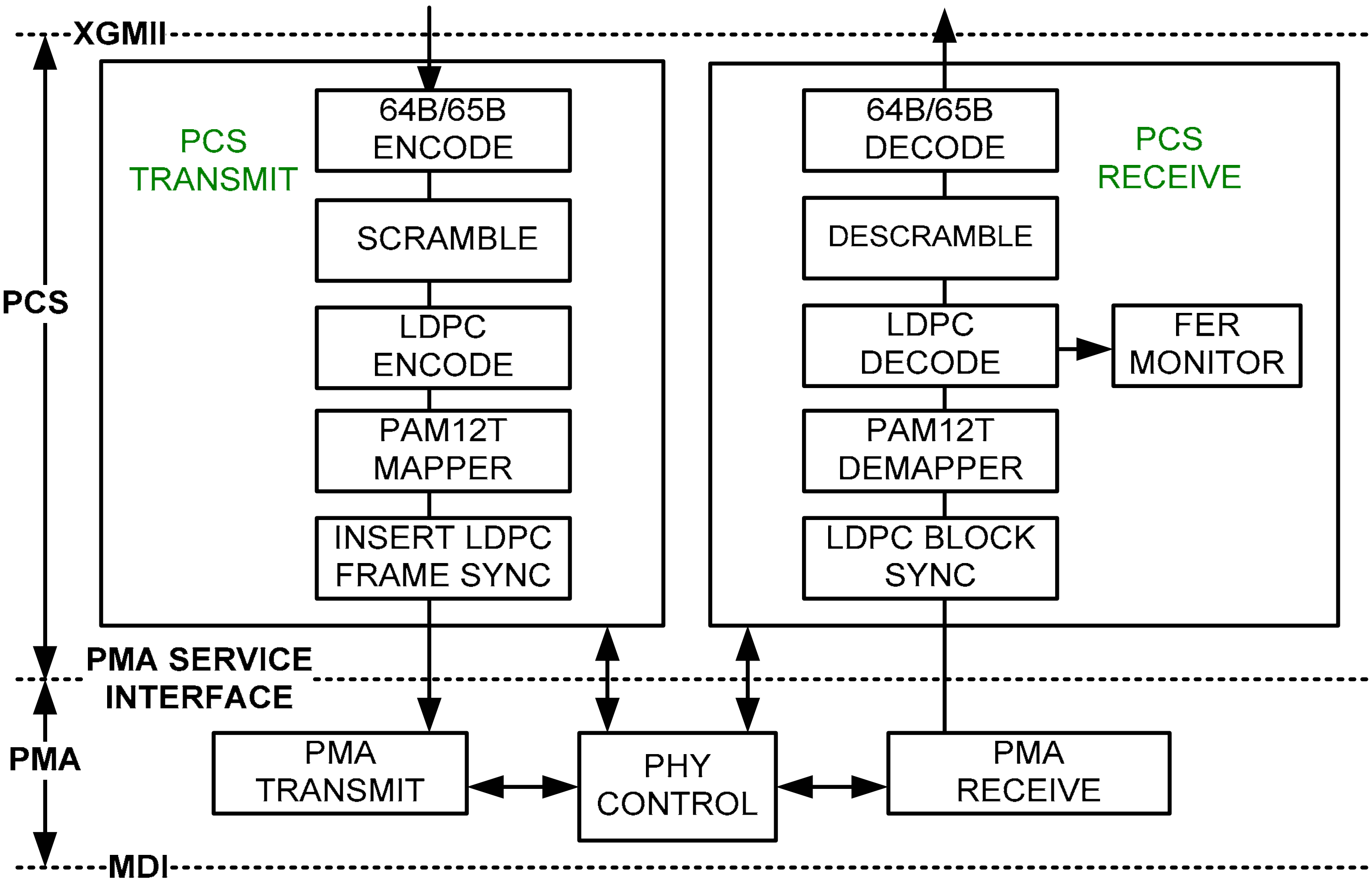
- Adaptive Rx equalizer removes residual ISI due to channel mismatch
  - Vendor dependent – precoding does not constrain Rx equalizer type (FFE, DFE, etc)

THP Start-up options

- Select “1 out of n” (extension of ungerboeck_1_0704.pdf).
  - Coefficients of THP feedback filter given by the channel SNR function
    - “Channel SNR” includes insertion loss, noise, residual Xtalk, filters, etc
  - Pole-zero models approximate long impulse response twisted pair channels with a smaller number of parameters
    - A 3-pole, 3-zero channel model accurately describes the worst case 100m cable model (powell_1_0304.pdf, ungerboeck_1_0704.pdf)
  - Select ‘1’ from ‘n’ fixed implementation-friendly precomputed ARMA(3,3) filters
- Programmable at start-up THP
  - Similar to HDSL2
- THP can be implemented as either FIR or IIR with specified tolerance (vendor specific)
- Need additional results to finalize THP design

Framing

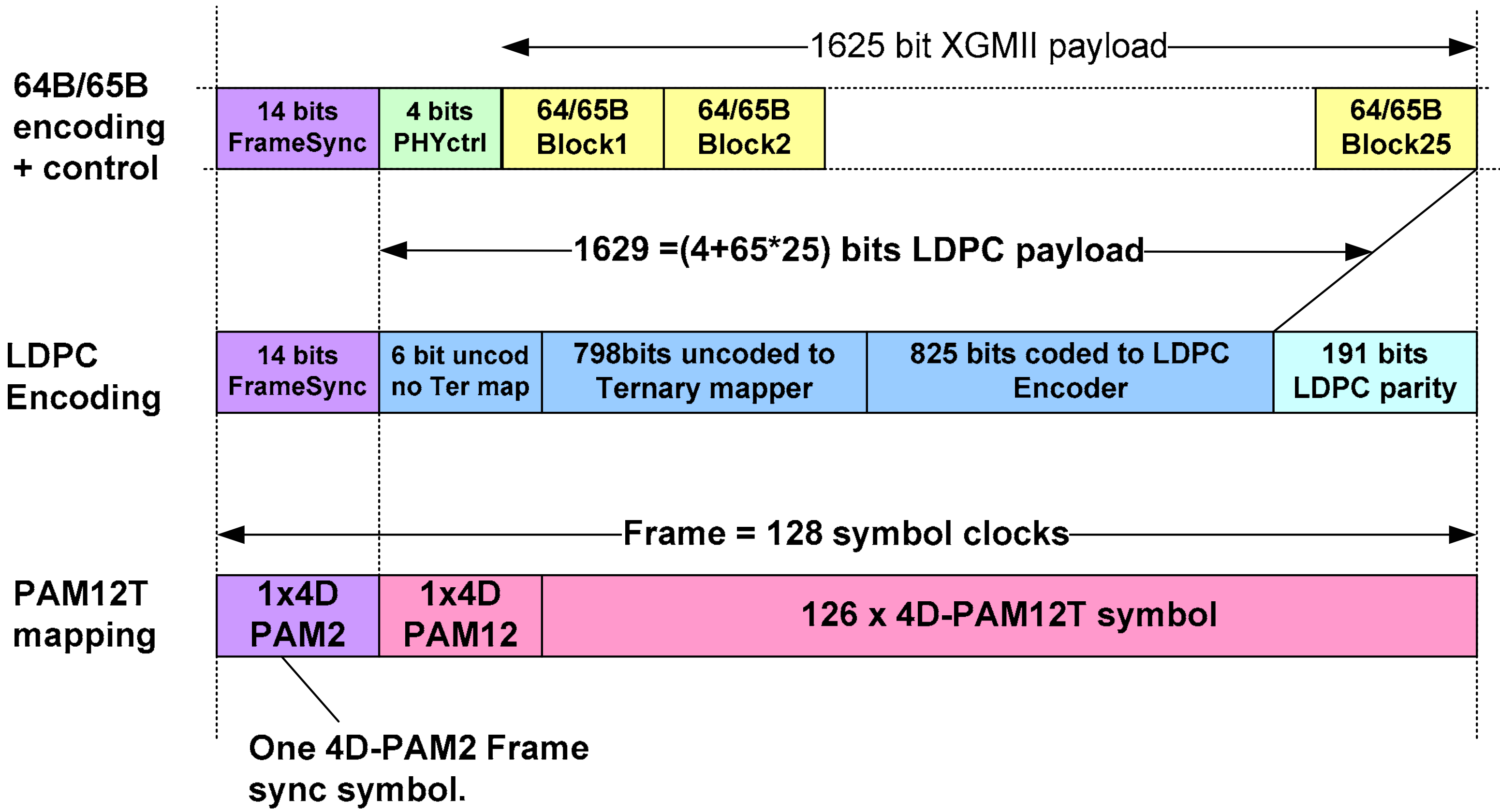
PCS Functional block



Framing and Control

- Convert XGMII to 64B/65B Code (based on 64B/66B Clause 49)
  - Aligned with LDPC Frame
    - LDPC frame sync provides 65B/65B code sync
  - Eliminates one sync bit (unnecessary with LDPC frame sync)
- Data payload of 25* 64 = 1600 bits
- LDPC block payload:
  - 1629 = 25x65B blocks + 4 PHYctrl
  - PHY control (4 bits): Optional for PHY status, SNR, etc. Up to 25Mbps of control.
- Frame has single LDPC block
  - 1x4D-PAM2 sync + 1x4D-PAM12 + 126x4D-PAM12T symbols
- Symbol rate: 10G/(1600/128) = 800MHz
- Symbol rate of 800MHz = 32* 25MHz
  - Easy to generate with standard xtals/oscillators with simple *N/M* PLL multiplication
  - Results in low jitter PLL
- This 800MHz framing can be easily modified to support LDPC(1024,821).

Framing and Control (cont'd)



LDPC to PAM12T mapping

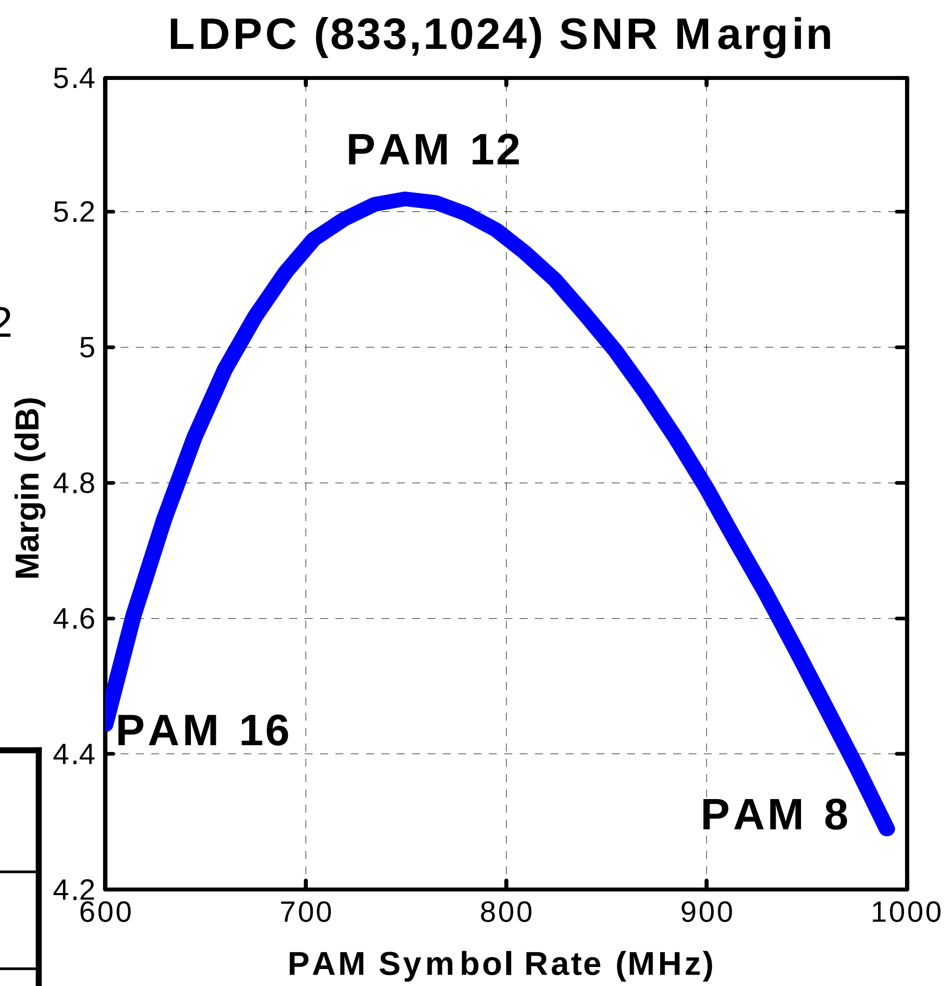
- PAM12T enhances dabiri_1_0304.pdf by additional 0.5 dB gain
- PAM12T mapping uses the following simple rules
  - LDPC encoder output levels Xn = {-3, -1, 1, 3}, n = 0:511
    - See Gray mapping in table below
  - Ternary encoder output: Tn = {-1, 0, 1}, n = 8:511
    - Converts 19 bits into 12 values Tn
    - Can use LUT, ESC encoding or base conversion (details in mcclellan_1_0904.pdf)
  - PAM12T mapping on wire A
    - A(k) = Xn+8*Tn, when n = 4k, k = 0:127
  - Similarly for wires B, C, and D when n = 4k+1, n = 4k+2 and n = 4k+3

LDPC_data_group <2n:2n+1> n=0:511 (coded bits)	**Xn (512 cosets)**
00	**-3**
01	**-1**
11	**1**
10	**3**

Performance

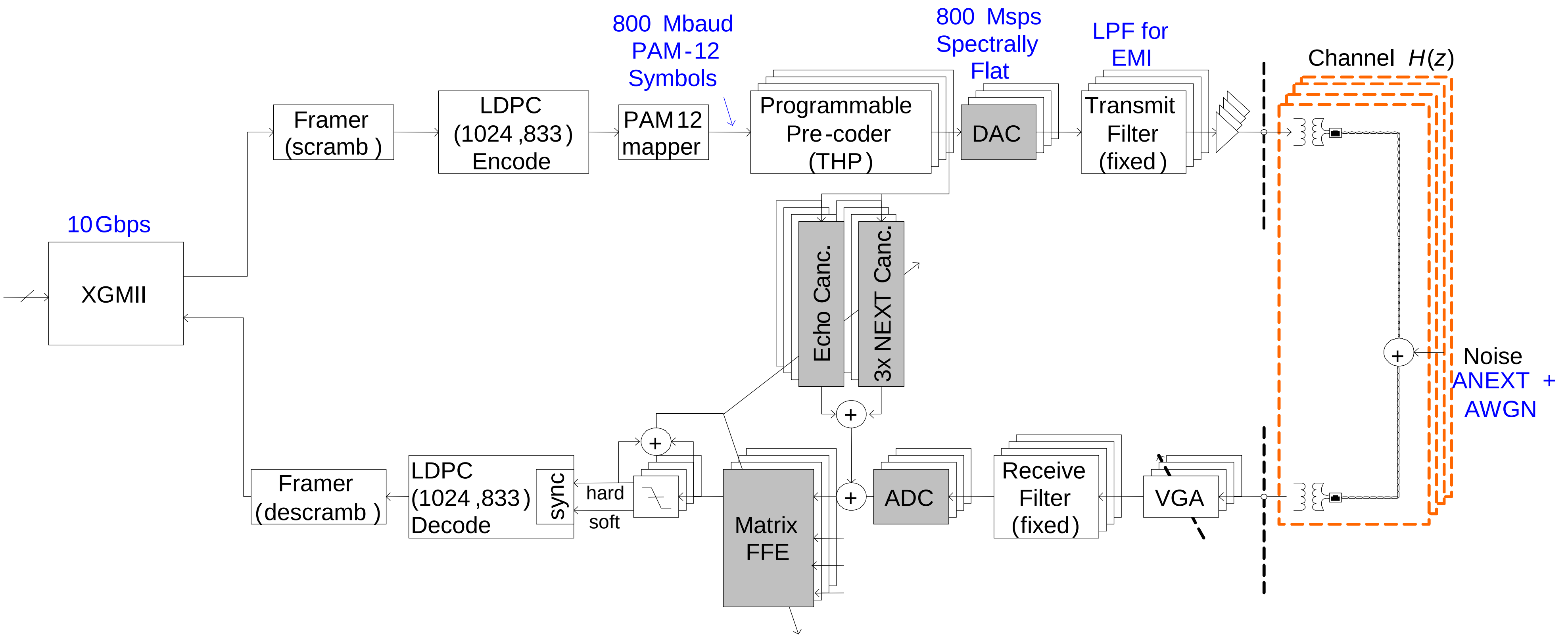
LDPC(1024,833) PAM12 Margin

- Largest Margin and Noise Immunity close to 800 MHz
- Assumptions
  - Model 3 (Cat6 IL, 100m)
  - 5 dBm Tx Power
  - LDPC required SNR=23.8 dB for BER<1e-12
  - Residual Impairments:
    - -150 dBm/Hz AWGN
    - 55 dB echo cancellation,
    - 40 dB NEXT cancellation
    - 25 dB FEXT cancellation



Performance margin	Model 1	Model 2	Model 3
SNR Margin	5.4dB	5.9dB	5.2dB
ANEXT Margin	7.3dB	6.2dB	7.4dB

Cancellers, FFE, ADC/DAC



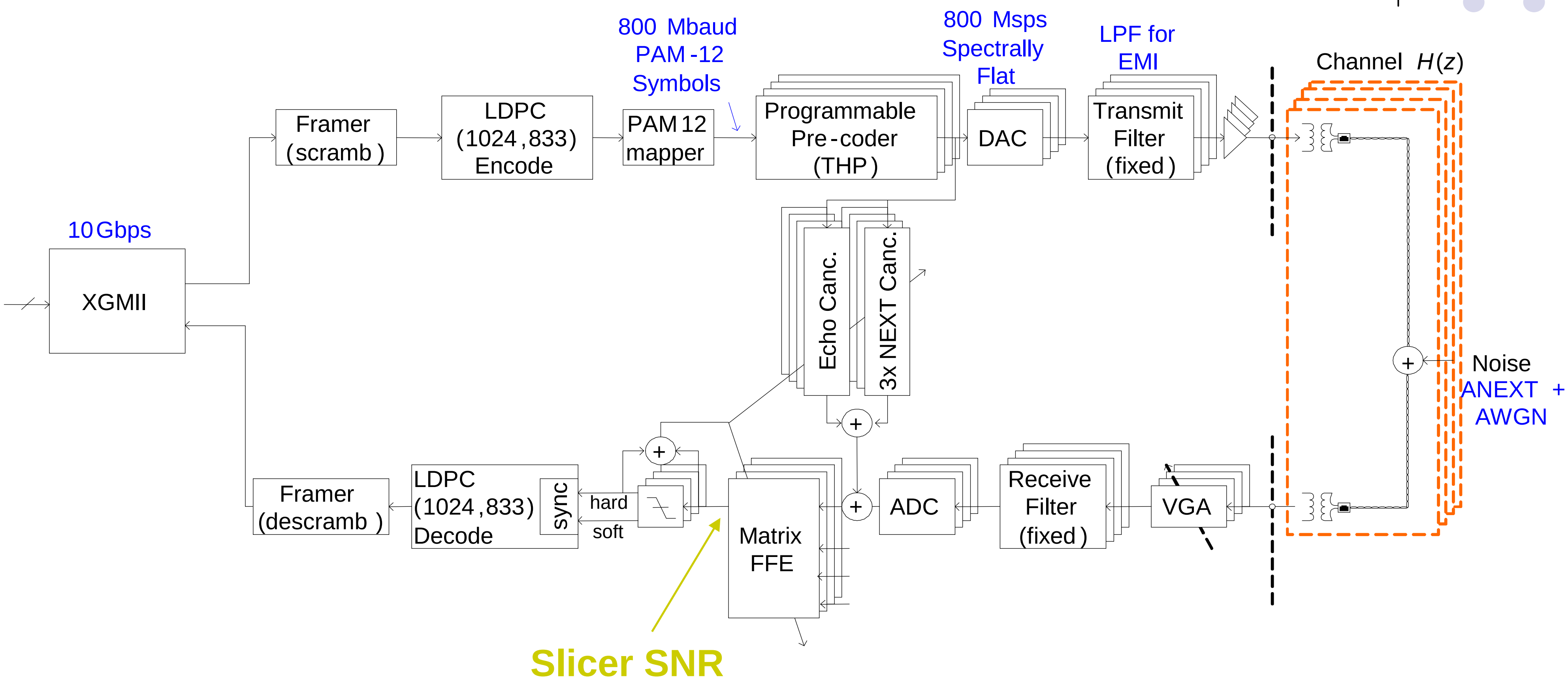
Implementation complexity is largely dominated by 4 echo cancellers, 12 NEXT cancellers, 4 equalizers and 12 FEXT cancellers, 4 DACs and 4 ADCs.

Example System Requirements

Echo Suppression	55 dB
NEXT Suppression	40 dB
FEXT Suppression	25 dB
ADC Resolution*	10 bits
DAC Resolution	10 bits
Timing Jitter	2.5 ps rms
Precoding Function	ARMA (3,3)
FFE span	64 taps

*** Assume ideal with 15 dB analog echo cancellation (see takatori_1_0304.pdf for feasibility)**

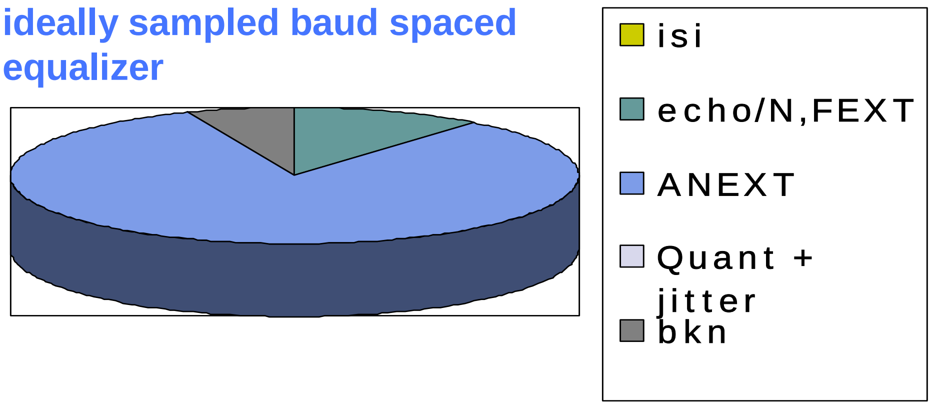
Overall Performance



Cable Model 3 Slicer SNR

100m "Cat 6e" PAM-12 Salz Solution

Optimum slicer SNR assuming ideal analog WMF + ideally sampled baud spaced equalizer



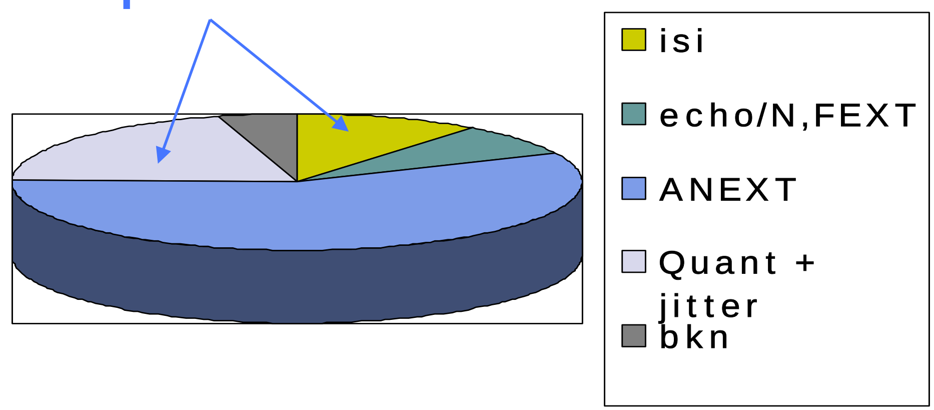
Total Slicer SNR = 28.9 dB

- **Required SNR = 23.8 dB**

∴ <u>5.2 dB design margin</u>

100m "Cat 6e" PAM-12 MMSE Solution

"Salz Analysis" ignores these components

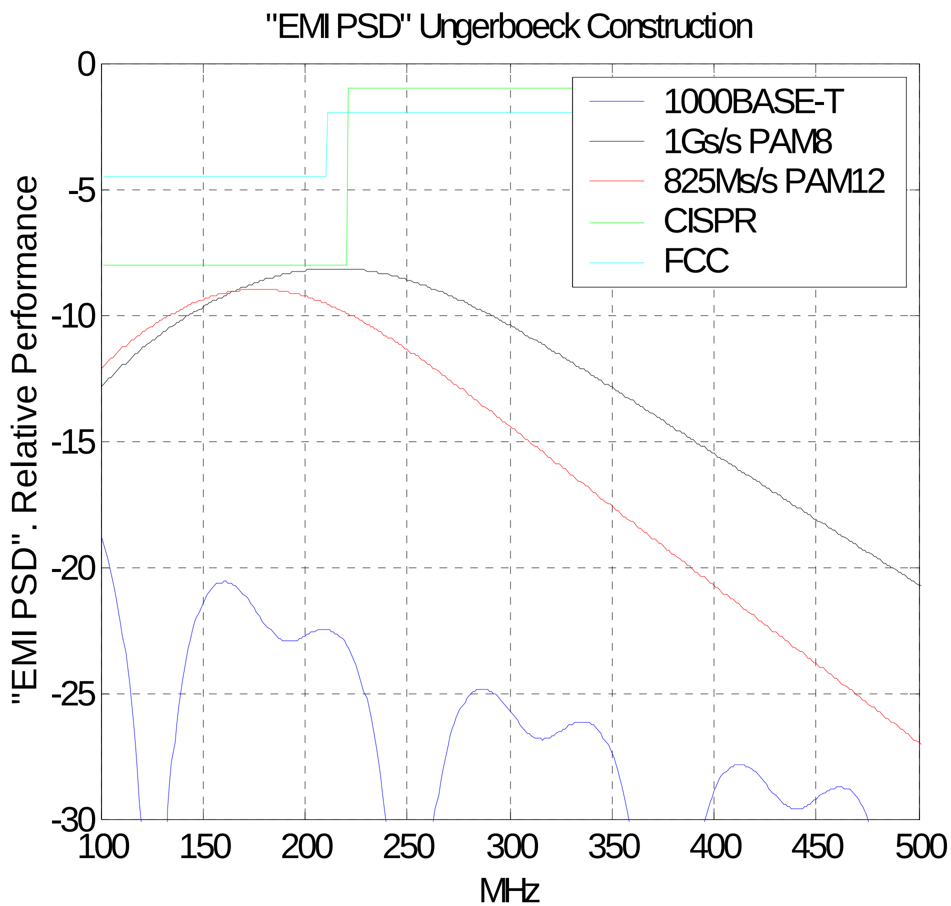


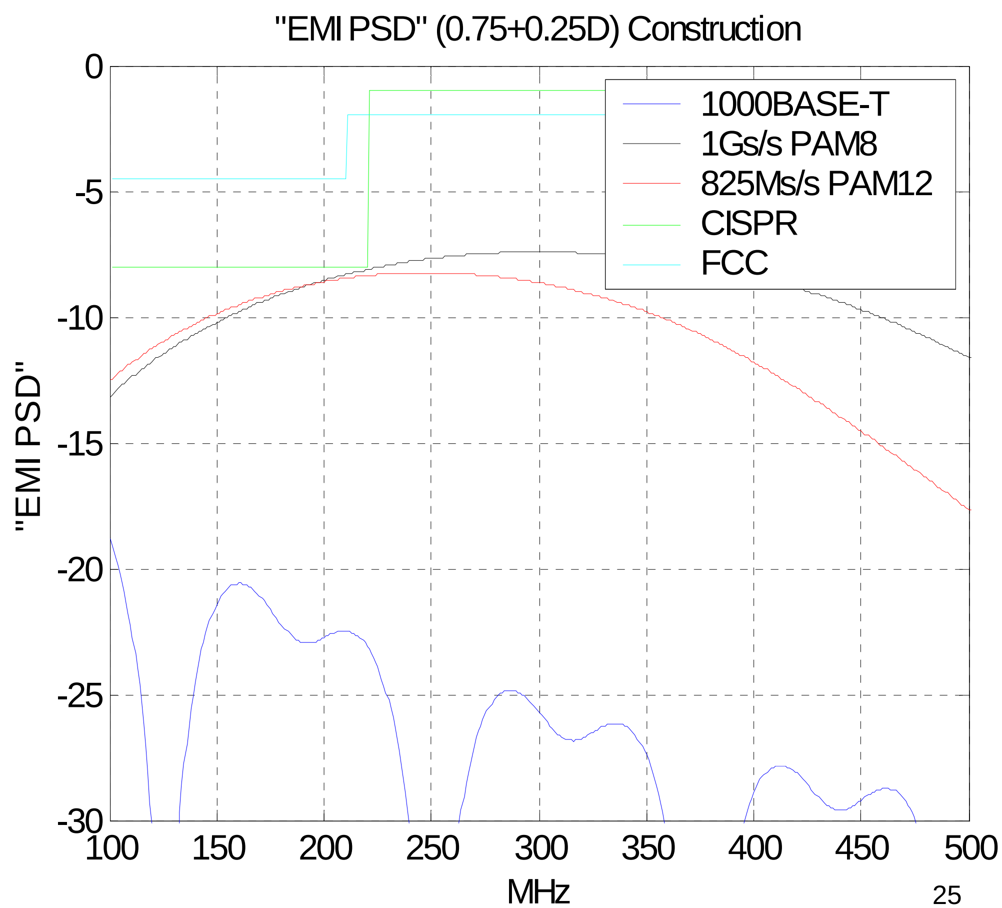
Total Slicer SNR = 26.6 dB

Note: isi+quant+jitter+bkn ~ -140 dBm/Hz

EMI PSD from Rao's "spectra.m" (ref: reflector email 7/22/04)

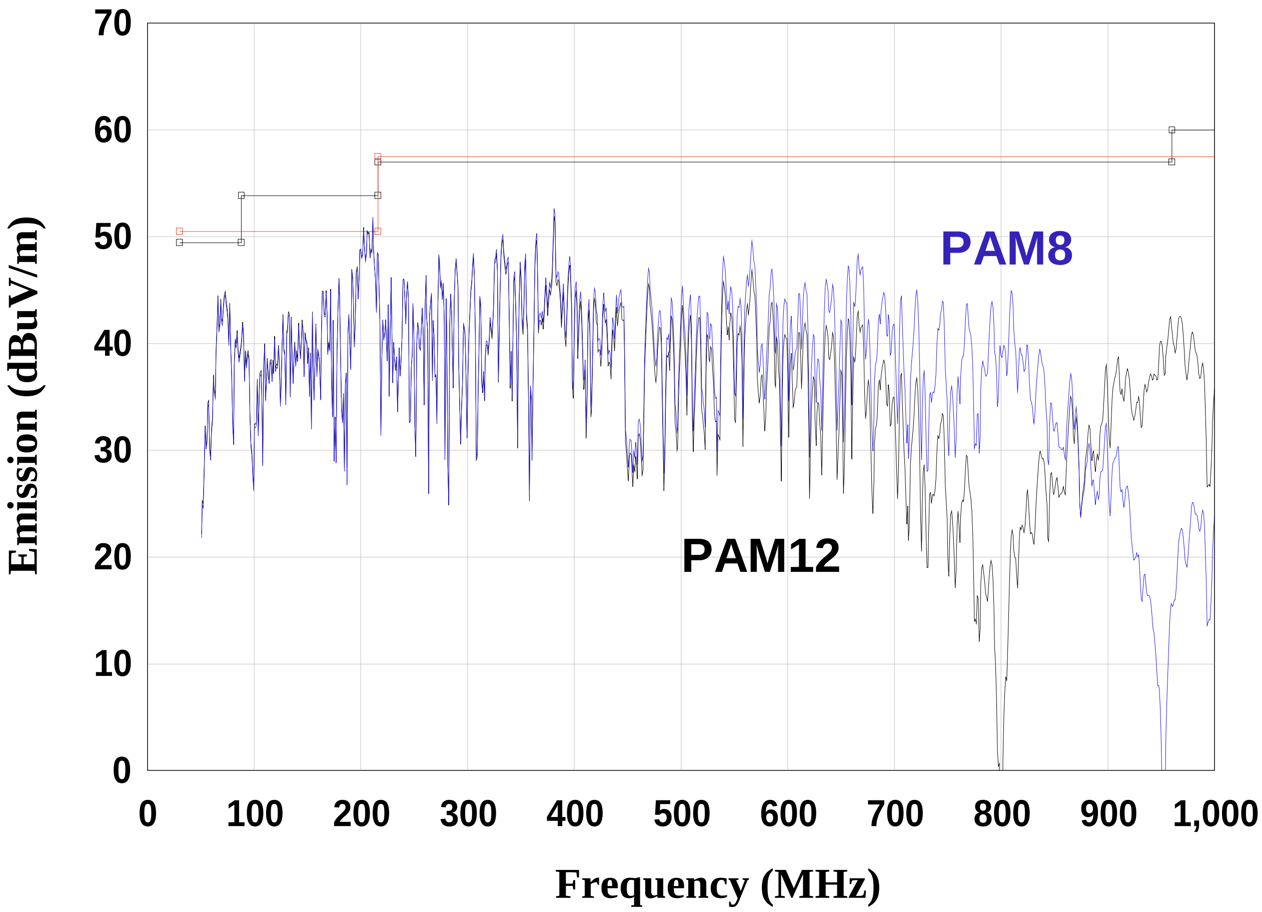
- PAM12T slightly better than PAM8 for typical low pass filters; either can be made to look slightly better than the other by tweaking LPFs
- Differences are minor; <u>not a compelling consideration re selection criteria</u>





EMI Comparison PAM8 vs PAM12

Predicted emissions based on measured transfer function



Proposal Summary

- *Framing and control:* 64B/65B with PAM2 sync headers
- *FEC code:* LDPC(1024,833), systematic
- *Modulation code:* Baseband PAM12-Ternary.
- *Equalization:* Start-up Selectable Tomlinson-Harashima precoder at Tx
- *Symbol rate:* 800MHz
- Benefits:
  - Achieves largest Salz SNR margin on worst case channels
  - Low Intrinsic latency of ~160ns
  - Lower symbol rate
    - Reduces power/size/cost
    - Reduces implementation complexity