Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanometer Regime—Part II: Quantitative Analysis

Seong-Dong Kim, *Member, IEEE*, Cheol-Min Park, *Member, IEEE*, and Jason C. S. Woo, *Senior Member, IEEE*

***Abstract*—Source/drain (S/D) series resistance components and device/process parameters contributing to series resistance are extensively analyzed using advanced model for future CMOS design and technology scaling into the nanometer regime. The total series resistance of a device is found to be very sensitive to the variations of the sidewall thickness, the doping concentration in the deep junction region, and the Schottky barrier height of silicide contact. A prediction of series resistance trends with technology generation indicates that silicide-diffusion contact resistance and overlap resistance will be major components in total series resistance of nanometer-scale CMOS transistors scaled according to the ITRS roadmap. The key factors for challenging scaling barriers related to parasitic resistance are quantitatively examined as a function of technology scaling and it is shown that the series resistance can be substantially reduced through controlling both abruptness of S/D junction profile and silicide Schottky barrier engineering.**

***Index Terms*—CMOS, high-κ dielectric, modeling, polysilicon gate depletion effect, scaling, series resistance, ultra shallow junction.**

I. INTRODUCTION

THE ultra-shallow source/drain (S/D) junction is an indispensable requirement to suppress short channel effect (SCE) in CMOS technology in the nanometer channel length regime and the design of S/D structure with ultra-shallow junction is susceptible to a high series resistance problem which degrades the ultimate intrinsic device performance [1], [2]. To overcome this scaling difficulty and identify the source of the high resistance problem, the extensive analyses for series resistance components and the device/process parameters of scaled CMOS contributing on series resistance are highly required. As reported in the previous paper [3], our advanced modeling takes important features of S/D structure of extremely short channel devices into account such as nonnegligible potential relationship in MOS accumulation region, lateral and vertical doping gradient effect of source/drain extension (SDE) junction and critical parameters of silicide diffusion contact system in addition to current behavior in ultrashallower SDE junction. The parasitic series resistance has been modeled by dividing into four components: SDE-to gate overlap resistance R_{ov}; S/D extension resistance R_{ext}; deep S/D resistance R_{dp}; and silicide-diffusion contact resistance R_{csd}. Each resistance component consists of the parallel or series combinations of subresistance components according to the carrier conduction path and junction structure profiles as illustrated in Fig. 1. This modeling approach provides very useful tool for physical examination of S/D series resistance components in detail as well as accurate estimation of them.

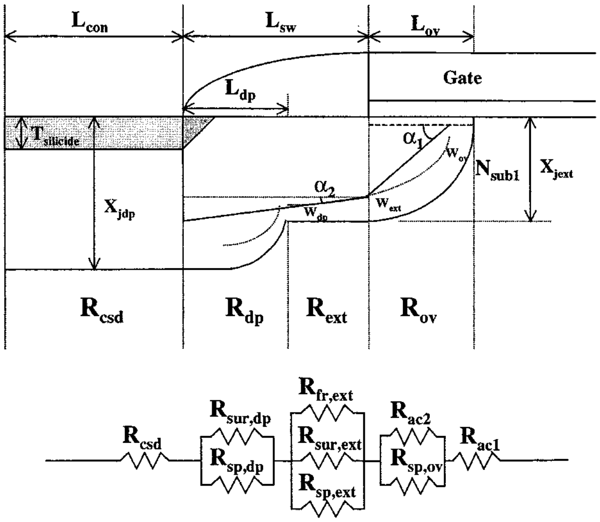


Fig. 1. Schematic representation of source/drain structure and parasitic series resistance components developed in advanced model.

In this paper, the advanced model is applied to investigate major resistance component and essential parameters impact on device optimization and scaling. We establish three CMOS transistors with different gate length in the nanometer scale based on projection of ITRS roadmap [4] to assess behavior of resistance components and parameters quantitatively as technology progresses and discuss about the key factors for challenging scaling barriers related to parasitic resistance.

II. IMPACT OF SOURCE/DRAIN PARAMETERS

The series resistances of CMOSFETs of which gate lengths are 100, 70, and 50 nm are calculated by use of the advanced model where the device structure and total resistance values were calibrated with the device simulations [3]. The device structure parameters of each technology are chosen according to the projections of ITRS road map [4] and listed in Table I. ITRS road map assumed the successful challenge of the scaling issues associated with the doping technology and the device dimension for the next generation devices, so that the

Manuscript received October 10, 2001; revised November 19, 2001. The review of this paper was arranged by Editor K. Shenai.

The authors are with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: woo@ee.ucla.edu).

Publisher Item Identifier S 0018-9383(02)02114-7.

TABLE I

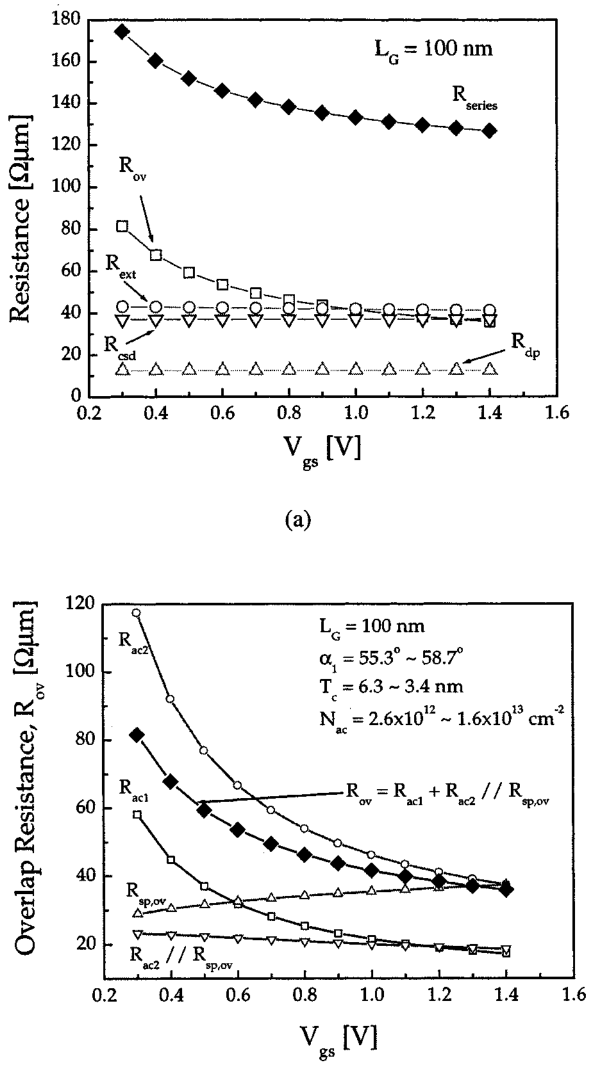
INPUT DEVICE STRUCTURE PARAMETERS CHOSEN ACCORDING TO THE PROJECTIONS OF ITRS ROAD MAP FOR THREE CMOS TECHNOLOGIES IN WHICH THE GATE LENGTHS ARE 100, 70, AND 50 nm

Gate length, L_G (nm)	100	70	50
Operating voltage, V_{DD} (V)	1.2	0.8	0.6
Gate dielectric thickness, T_{ox} (nm)	2.0	1.5	1.0
Sidewall length, L_{sw} (nm)	100	60	40
Overlap length, L_{ov} (nm)	20.5	12.5	9.5
Deep junction length, L_{dp} (nm)	55	36	25
SDE junction depth, X_{jext} (nm)	34.5	26.5	16.5
Deep junction depth, X_{jdp} (nm)	111	65	49
Silicide thickness, $T_{silicide}$ (nm)	30	25	15
Peak SDE doping, $N_{max,ext}$ (cm^{-3})	7.0×10^{19}	1.2×10^{20}	1.5×10^{20}
Peak Deep doping, $N_{max,dp}$ (cm^{-3})	3.0×10^{20}	4.0×10^{20}	6.0×10^{20}
Substrate doping, N_{sub1} (cm^{-3})	1.5×10^{18}	2.0×10^{18}	3.0×10^{18}
Poly doping, N_p (cm^{-3})	3.0×10^{20}	1.2×10^{20}	6.0×10^{20}

TABLE II

SELECTED OUTPUT PARAMETERS CALCULATED BY ADVANCED MODEL AT EACH OPERATING GATE VOLTAGE FOR THREE NMOS DEVICES WITH DIFFERENT TECHNOLOGIES

Gate length, L_G (nm)	100	70	50
Channel thickness, T_c (nm)	3.77	3.95	3.83
Accumulation carrier concentration, N_{ac} (cm^{-2})	1.16×10^{13}	1.02×10^{13}	1.11×10^{13}
Spreading angle, α_1 (degree)	58.4	63.5	54.2
Spreading angle, α_2 (degree)	6.9	11.5	14.9
SDE sheet resistance, $R_{sh,ext}$ (Ω/sq)	664	561	713
Depletion width, W_{ov} (nm)	6.37	4.29	3.46
Depletion width, W_{ext} (nm)	7.83	6.13	4.30
Depletion width, W_{dp} (nm)	2.38	1.24	0.31
Specific contact resistivity, ρ_c (Ωcm^2)	4.4×10^{-8}	3.0×10^{-8}	1.8×10^{-8}
Lateral SDE abruptness (nm/dec)	12.28	7.03	5.59



(a)

(b)

Fig. 2. (a) Series resistances and their components of 100 nm-gate-length NMOSFET as a function of gate voltage estimated by advanced model. (b) Calculated resistance components of the overlap region.

parameters used in this work are based on the extremely heavily doped, ultrashallow SDE junction and properly scaled lateral and vertical S/D dimensions. The selected output parameters calculated by model at each operating voltage for three NMOS technologies are also listed in Table II.

Fig. 2(a) shows source series resistances and their components of 100 nm-gate-length NMOSFET as a function of supply gate voltage estimated by advanced model. All the resistance components except $R_{\rm dp}$ show almost the same contribution to total series resistance in 100 nm gate length technology. As seen in experimentally and simulation study [5], [6], the model predicts that the decrease of series resistance with $V_{\rm gs}$ incurred by overlap resistance reduction due to enhanced carrier accumulation. The behavior of overlap resistance components are depicted in Fig. 2(b). As $V_{\rm gs}$ increases, accumulation carrier density increases in nearly exponential manner, so that $R_{\rm ac1}$ and $R_{\rm ac2}$ sharply decrease. On the contrary, the parallel combination of $R_{\rm ac2}$ and $R_{\rm sp,ov}$ is not changed much with $V_{\rm gs}$, because the current spreading into the bulk exert much influence on sub-resistance component over whole $V_{\rm gs}$ ranges. This results indicate that $R_{\rm ac1}$ plays an important role in determining the voltage-dependent overlap resistance characteristics.

The polysilicon gate depletion effect (PDE) is another limitation for nanoscale short channel devices since it increases equivalent thicknesses of aggressively scaled oxide layers below 2 nm and degrades device current performance. The series resistance is also affected by PDE as calculated by advanced model in Fig. 3. The overlap resistance increases with decreasing poly-doping concentration and is more degraded in lower SDE doping concentration due to the pronounced PDE [7].

Because of large direct-tunneling current of extremely thin gate oxide, a high dielectric constant material is being attempted to be employed in gate stack system or sidewall spacer [8], [9]. The effect of high-κ sidewall material on series resistance is also demonstrated in Fig. 4. In Fig. 4, it can be found that the use of very high-κ dielectric sidewall significantly induces the

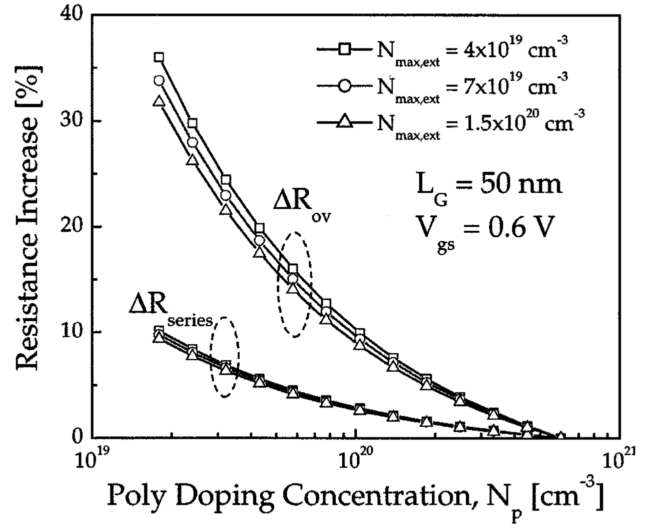


Fig. 3. Poly-depletion effect on series resistance for different poly-doping and SDE doping concentration obtained by advanced model.

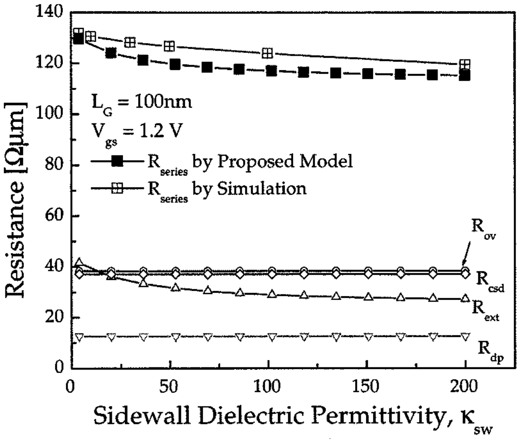


Fig. 4. Effect of high-κ sidewall material on the series resistance. The use of high-κ dielectric sidewall reduces the extension resistance by inducing the carrier accumulation in surface extension region due to the increased fringing field.

carrier accumulation in surface extension region due to the increased fringing field, resulting in reduction in $R_{\rm ext}$ and hence $R_{\rm series}$ as reported in [9], while this may invoke the increase of gate-to-S/D capacitance problem.

Fig. 5 shows the sensitivity of total series resistance to process/device parameters calculated by the model when the process/device parameters are varied up to $\pm 15\%$. The total series resistance is very sensitive to even small variations of the Schottky barrier height, the sidewall length, $L_{\rm sw}$ and doping concentration in the deep junction region $N_{\rm max,dp}$.

III. ANALYSIS ON CMOS SCALING

In order to find and overcome the series resistance obstacle in future CMOS scaling, it is necessary to understand the relative contributions of each resistance component to the total series resistance. Fig. 6(a) and (b) show the relative contributions of each resistance component to the total series resistance as a function of technology scaling calculated by the model for conventional planar type NMOS and PMOS, respectively. The device dimensions and doping concentrations of each technology are assumed to be scaled down according to ITRS roadmap as listed in Table I, and the same scaled device parameters are employed for both NMOS and PMOS except physical parameters related to silicide Schottky contact and carrier mobility. The Schottky barrier height of midgap-level silicide contact material is assumed for all technologies and are fixed at 0.6 eV and 0.51 eV for NMOS and PMOS, respectively. It should be noted from Fig. 6 that the silicide-diffusion contact resistance $R_{\rm csd}$ and the overlap resistance $R_{\rm ov}$ are expected to be dominant resistance components for future technology scaling. The sum of their contributions on total series resistance is about 70% at 50 nm gate length. The important trends are that the contribution of the silicide-diffusion contact resistance increases as the technology shrinks, while the overlap resistance is almost at the same level for all technologies. In particular, the overlap resistance component is more severe in the case of PMOS due to the relatively poor accumulation layer mobility. Fig. 6 suggests that much significant effort for S/D engineering should be concentrated on the SDE-to-gate overlap and the contact region.

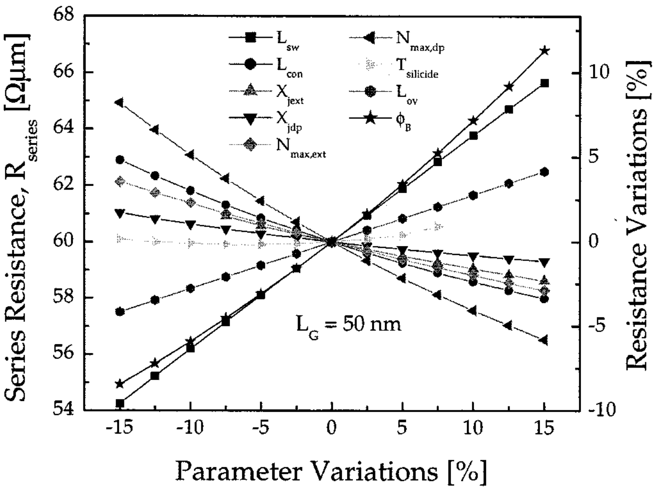
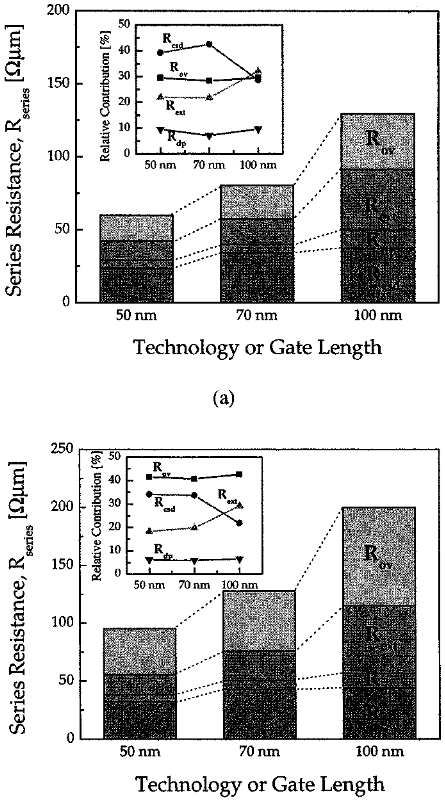


Fig. 5. Sensitivity analysis of series resistance to the process/device parameters. The sidewall thickness ($L_{\rm sw}$), the doping concentration in the deep junction region ($N_{\rm max,dp}$), and Schottky barrier height (ϕ_B) of silicide material are the most sensitive process/device parameters to series resistance.

In order to optimize S/D structure to obtain the best possible electrical performance as device is scale down, the extensive and quantitative analysis on the key optimization parameters of each series resistance component is essential. The device parameters seriously contribute to series resistance are examined by analyzing three important resistance components, $R_{\rm ov}$, $R_{\rm ext}$, and $R_{\rm csd}$ as a function of technology as follows.

The first component is the SDE-to-gate overlap resistance. Fig. 7 shows component analysis of $R_{\rm ov}$ scaling as a function of technology gate length. Among the resistance components, $R_{\rm ac1}$ is the most troublesome component in scaling of $R_{\rm ov}$. To find out serious device parameters impact on $R_{\rm ov}$, the overlap resistance and its component variations are calculated and plotted as a function of lateral abruptness of SDE profile for different SDE doping in Fig. 8. The inset of Fig. 8 illustrates the lateral doping profile variation as a function of the overlap distance when the lateral abruptness is kept constant of



(a)

(b)

Fig. 6. Relative contributions of resistance components to the total series resistance as a function of technology scaling calculated by advanced model. The device parameters of each technology are scaled down according to ITRS roadmap. (a) NMOS and (b) PMOS.

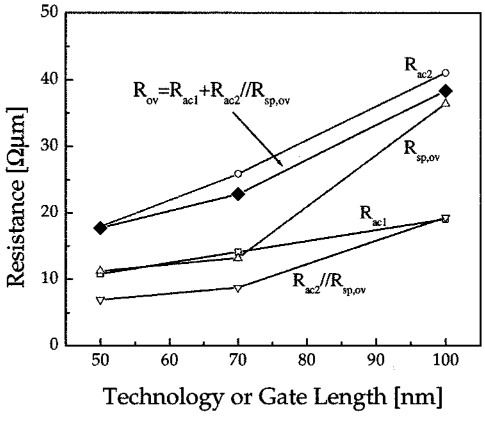


Fig. 7. Overlap resistance $(R_{\rm ov})$ and its component variation as a function of gate length. Accumulation resistance $(R_{\rm ac1})$ is most troublesome component to reduce.

10 nm/dec. As the lateral abruptness decreases, the resistance components of the overlap region decrease depending on lateral abruptness of SDE profile, but show a little differences with the maximum doping concentration of SDE. This result suggests that $R_{\rm ov}$ scaling can be mainly determined by the lateral junction profile slope rather than its maximum doping concentration which is primarily limited by dopant solid-solubility and the device SCE due to difficulty of junction depth control.

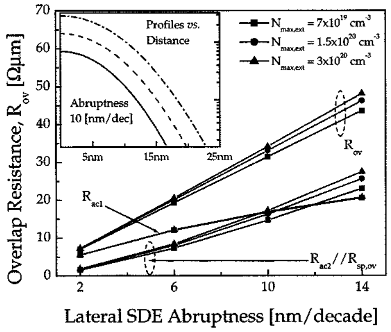


Fig. 8. Overlap resistance $(R_{\rm ov})$ and its component variation as a function of lateral SDE abruptness. The inset illustrates the lateral doping profile variation as a function of the overlap distance when the lateral abruptness is kept constant of 10 nm/dec.

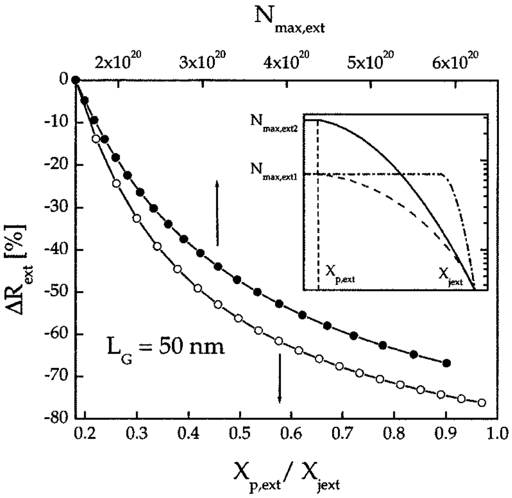
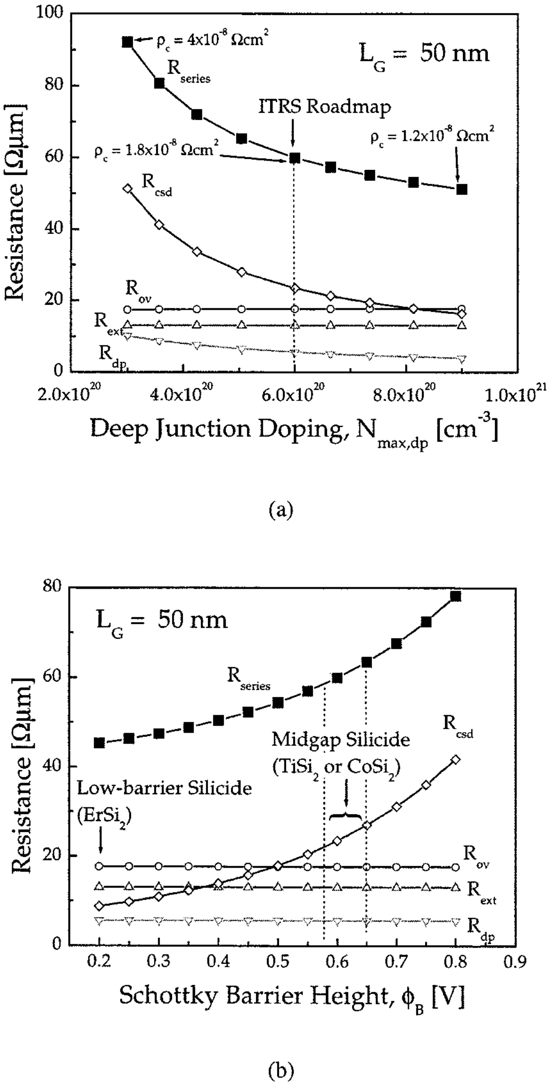


Fig. 9. Effect of vertical abruptness of SDE junction profile on series resistance for the same junction depth $(X_{j{\rm ext}})$. The inset illustrates the variation of doping profile depending on the surface doping or $X_{p,{\rm ext}}$ location.

The importance of the abruptness of SDE junction profile is also governed in $R_{\rm ext}$ reduction as can be seen in Fig. 9. The inset of Fig. 9 illustrates variation of doping profiles depend on the surface doping or $X_{p,{\rm ext}}$ location. The increase of vertical abruptness with increasing $X_{p,{\rm ext}}$ has a significant effect on $R_{\rm ext}$ reduction as compared to that of surface extension doping. The extension resistance can be reduced down to around 80%, if the box-shaped vertical junction profile is achieved. But the large increase of surface doping concentration of SDE region may be detrimental to short channel performance.

The silicide-diffusion contact resistance is the most serious component to reduce as discussed in Fig. 6. The controlling of specific contact resistivity ρ_c will be essential for $R_{\rm csd}$ reduction as given by model formula [3] . In this model, the specific contact resistivity can be obtained from the input parameters based on the assumptions of final Gaussian doping concentration of the deep junction region and the silicide materials with the barrier height of the midgap such as $TiSi_2$ and $CoSi_2$. The effective contact lengths determined by the edge of the sidewall and the isolation in the longitudinal direction are found to be smaller than calculated transfer lengths for all technologies. The numerical simulation have shown that the one-dimensional (1-D)



(a)

(b)

Fig. 10. (a) Resistance variation as a function of deep junction doping concentration. (b) Resistance variation as a function of Schottky barrier height. The percentage of $R_{\rm csd}$ contribution can be reduced remarkably by Schottky barrier height lowering technique using alternative low barrier height metal (e.g., $ErSi_2$ for NMOS) instead of midgap (0.57–0.65 eV) silicide metal.

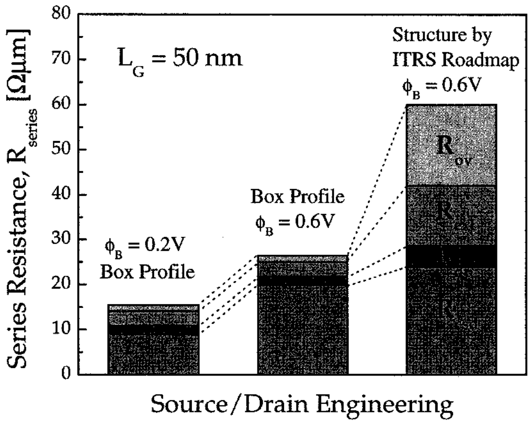


Fig. 11. Resistance contributions of each resistance component to the total series resistance in sub-50 nm NMOS according to S/D engineering variation. $R_{\rm series}$ value can be reduced to 35% of that of roadmap structure if box-shaped S/D junction and low Schottky barrier height material will be successfully challenged.

transmission line model (1-D-TLM) characterizes $R_{\rm csd}$ variation quite well when the contact size is smaller than the transfer length [10]. The calculated specific contact resistivity of the silicon/silicide interface is on the order of $10^{-8}\ \Omega\cdot{\rm cm}^2$ and negligible for larger channel length devices, whereas, in the case of nanoscale devices, it makes a relatively large contribution to total series resistance even with heavily doped deep junction as shown in Fig. 10(a). To reduce $R_{\rm csd}$ contribution in next generation technology, it is necessarily required that maximizing the active dopant concentration at the silicide/Si interface or minimizing Schottky barrier height to obtain an acceptable specific contact resistivity as evaluated in Fig. 10. In Fig. 10(b), it is observed that the percentage of $R_{\rm csd}$ contribution can be reduced remarkably to the value below that of $R_{\rm ov}$ and $R_{\rm ext}$ even with a small reduction of Schottky barrier height, while the maximizing doping concentration has a fundamental limitation of solid solubility. Although technologically problematic yet, the Schottky barrier height lowering technique by using alternative metal having lower barrier height of 0.2–0.25 eV, e.g., $ErSi_2$ for NMOS and $PtSi_2$ for PMOS [11] or using lower bandgap layer like $Si_{1-x}Ge_x$ films [12] will be a possible strategy for successful CMOS scaling.

Fig. 11 shows the expected trend of the series resistance reduction by S/D engineering on the basis of 50 nm device with conventional planar type NMOS structure predicted by advanced model, when the progressive engineering of both the S/D junction abruptness and Schottky barrier height are successfully achieved. More than 50% reduction in series resistance will be expected and especially, the resistance components related to ultra-shallow S/D junction will be reduced dramatically by box-shaped SDE and deep junction profile.

IV. CONCLUSION

The advanced physical model is employed to analyze the effect of S/D device parameters on series resistance contribution and predicts series resistance reduction trend with CMOS technology generation below 100 nm gate length. The model well characterizes nanoscale CMOS structure and resistance characteristics including polysilicon depletion effect and high-κ sidewall spacer effect. It is shown that the sidewall thickness, the doping concentration in the deep junction region, and the Schottky barrier height of silicide material are the most sensitive process/device parameters to series resistance variation. The series resistance trend with respect to technology scaling predicts the sum of silicide-diffusion contact and overlap resistance contributions on total series resistance will be about 70% at 50 nm gate length and the percentage of the silicide-diffusion contact resistance contribution increases as the technology shrinks. The modeling analysis suggests that advanced S/D engineering focusing on highly abrupt SDE junction profile and lower Schottky barrier silicide contact should be challenged for successful CMOS technology scaling.

REFERENCES

[1] Y. Taur, C. H. Wann, and D. J. Frank, "25 nm CMOS design considerations," in *IEDM Tech. Dig.*, 1998, pp. 789–92.

[2] J. D. Plummer and P. B. Griffin, "Material and process limits in silicon VLSI technology," *Proc. IEEE*, vol. 89, pp. 240–258, Mar. 2001.

[3] S. D. Kim, C.-M. Park, and J. C. S. Woo, "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime—Part I: Theoretical derivation," *IEEE Trans. Electron Devices*, vol. 49, pp. 457–466, Mar. 2002.

[4] *The National Technology Roadmap for Semiconductors (ITRS)*

[5] S. Biesemans, S. Kubicek, and K. D. Mayer, "Test structure to investigate the series resistance components of source/drain structure," *IEEE Electron Device Lett.*, vol. 18, pp. 477–479, Oct. 1997.

[6] K. K. Ng and W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 965–972, July 1986.

[7] C.-L. Huang and N. D. Arora, "Measurements and modeling of MOSFET I–V characteristics with polysilicon depletion effect," *IEEE Trans. Electron Devices*, vol. 40, pp. 2330–2337, Dec. 1993.

[8] B. Cheng, M. Cao, R. Rao, A. Inani, P. V. Voorde, W. M. Greene, J. M. C. Stork, Z. Yu, P. M. Zeizoff, and J. C. S. Woo, "The impact of high-κ gate dielectric and metal gate electrodes on sub-100 nm MOSFET's," *IEEE Trans. Electron Devices*, vol. 46, pp. 1537–1544, July 1999.

[9] D. L. Kencke, W. Chen, H. Wang, S. Mudanai, Q. Ouyang, A. Tasch, and S. K. Banerjee, "Source-side barrier effects with very high-κ dielectrics in 50 nm Si MOSFET's," in *57th Annu. DRC Dig.*, 1999, pp. 22–23.

[10] Y.-S. Chieh, A. H. Perera, and J. P. Krusius, "Series resistance of silicided ohmic contacts for nanoelecronics," *IEEE Trans. Electron Devices*, vol. 39, pp. 1882–1888, Aug. 1992.

[11] J. Kedzierski, P. Xuan, E. H. Anderson, J. Boker, T.-J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFET's for the 20 nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp. 57–60.

[12] H.-J. Huang, K.-M. Chen, C.-Y. Chang, L.-P. Chen, G.-W. Huang, and T.-Y. Huang, "Reduction of source/drain resistance and its impact on device performance for PMOS transistors with raised $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ source/drain," *IEEE Electron Device Lett.*, vol. 21, pp. 400–402, Sept. 2000.

Seong-Dong Kim (S'94–M'97) was born in Chonan, Korea, in 1967. He received the B.S., M.S., and Ph.D. in electrical engineering from Seoul National University, Seoul, Korea, in 1990, 1992, and 1996, respectively. His graduate research was focused on the power semiconductor devices and ICs.

From 1996 to 1999, he was with the System IC Research and Development Center, Hyundai Electronics Industries, Seoul, Korea, where he engaged in the research and development of submicron CMOS technologies, CMOS image sensors, and high voltage CMOS-DMOS ICs. In December 1999, he joined the Department of Electrical Engineering, University of California, Los Angeles, as a Research Engineer, where he has been conducting research on the physics, technology, and modeling of nanometer-scale CMOS devices. His research interests include the design, fabrication, and modeling of CMOS VLSI technologies, SOI devices, and power semiconductor devices.

Cheol-Min Park (S'96–M'01) was born in Seoul, Korea, in 1971. He received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, in 1994 and 1996, respectively, where he is currently pursuing the Ph.D. degree in the School of Electrical and Computer Engineering.

His current research interests are in electrical and structural properties of poly-Si thin-film transistors.

Jason C. S. Woo (S'83–M'87–SM'97) received the B.A.Sc. (Hons.) degree in engineering science from the University of Toronto, Toronto, ON, Canada, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1982 and 1987, respectively.

In 1987, he joined the Department of Electrical Engineering, the University of California, Los Angeles, where he is currently a Professor. His research interests are in the physics and technology of novel device and device modeling, and he has authored more than 100 papers in technical journals and the refereed conference proceedings in these areas.

Dr. Woo served on the IEEE IEDM Program Committee from 1989 to 1990 and from 1994 to 1996, and was Publicity Vice Chairman in 1992 and the Publicity Chairman in 1993. He has been the Workshop Chairman and a Technical Committee Member of the VLSI Technology Symposium since 1992. He has served on the committee for the IEEE SOI Conference since 1995. He received a Faculty Development Award from IBM from 1987 to 1989.