

# SCALING TRENDS FOR THE ON CHIP POWER DISSIPATION

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## 1. ABSTRACT

Power is increasingly becoming the bottleneck for the design of high performance microprocessors. It is essential to analyze how the various components of power are likely to scale in the future, thereby identifying the key problematic areas. Toward this end, a complete model for the on-chip power dissipation is presented, followed by the investigation of power breakdown at future technology nodes.

## 2. INTRODUCTION

Performance of high-end microprocessors is increasingly getting constrained by the total power dissipation on the chip. Key design decisions are already being governed by the power budget, apart from delay and area. With the rapid increase in transistor density and speed, power is likely to be the performance bottleneck in the future. It is, therefore, imperative to characterize how the various power dissipation components scale. In this work, we put together a complete model for the total power dissipated on the chip. Using the data from the International Technology Roadmap for Semiconductors (ITRS) [1], various components of power are then evaluated at the future technology nodes. A complete breakdown of power dissipation at the 50nm node is presented.

## 3. POWER DISSIPATION MODELS

The total power dissipation on the chip can be divided into four classes: interconnects, logic, memory, and clock distribution and latches. Clock distribution and latches are considered separately owing to the high duty cycle of the clock signal. For the logic and memory, power can further be classified as being dynamic power or static (leakage power). The modeling of leakage power would be identical for logic and memory.

### A. Interconnect power dissipation model

Only the interconnects that are part of the logic are modeled, as memory is quite different and can not be modeled using the stochastic wirelength distributions [2]. Local, intermediate (semi-global) and global tiers need to be considered separately. This is because global clocks and local clocks are different. Further, to minimize delay, global lines also contain repeaters that need to be taken into account. We use the stochastic wirelength distribution developed by [3]. A Rent's exponent of 0.55 is assumed [4]. The maximum length of the wire in the local tier is

obtained by allocating it no more than 25% of the local clock cycle [5]. The demarcation between semi-global and global wiring tiers is obtained by using the notion of isochronous regions, which are clock domains reachable by the local clock in a single clock cycle [6,7]. These isochronous regions are connected by global wires, running at the global clock frequency. For the global lines, based on expressions for optimal sizing and spacing [8], repeater capacitance is also calculated and added to the global wire capacitance. Once the capacitance is calculated, the power dissipation for each tier is given by:

$$P_{int} = s_w C_{int} V^2 f_c$$

Where  $C_{int}$  is the interconnect capacitance, and  $s_w$  is the switching activity. Switching activity is assumed to be 0.15 for the global and semi-global interconnects [9], and 0.1 for local interconnects. Local interconnects have lower switching activity because switching activity is highest at the higher levels and reduces as the depth of architecture increases.

### B. Logic power dissipation model

The leakage power in logic will be modeled in a later section. The dynamic power in logic is modeled as

$$P_{logic} = 3s_w N_{logic} W_{avg} C_{trans} V^2 f_c \left(1 - \frac{1}{f_{ld}}\right)$$

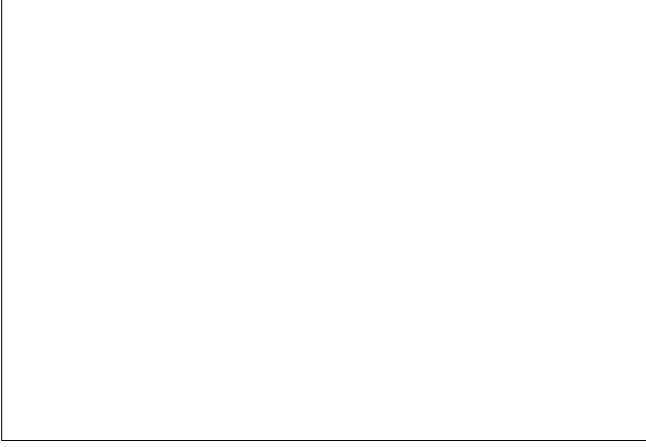
Here,  $N_{logic}$  is the number of logic gates,  $W_{avg}$  is the average transistor size at the input of the gate, and  $C_{trans}$  is the gate capacitance per unit length for the transistor.  $f_{ld}$  is the average logic depth, taken to be 12 [10]. The width to length ratio of an average transistor is taken to be 12 [11] and  $W_{avg}$  is calculated accordingly.  $C_{trans}$  stays approximately constant at  $1.75 fF/\mu m$  [12]. Switching activity for logic is the same as for local interconnects.

### C. Memory power dissipation model

The dynamic power dissipation in memory occurs only during reads and writes. The dominant part of the power dissipation is the charging and discharging of the huge capacitance of the *bit/bit* wires and the transistors connected to these wires [13]. Expression for this is derived in [14] and is modified for our purposes to give the following:

$$E_{mem} = \frac{\sqrt{N_{mem}}}{2} (C_{int} l_{col} + \sqrt{N_{mem}} C_{diff}) V_{dd} V_{swing}$$

The above expression assumes a square layout for memory, and  $N_{mem}$  is the total number of transistors in the memory.  $l_{col}$  is



**Fig. 1.** Grid based clock distribution, assumed in this work

the column height, which is the square root of memory area in this case. Memory area is calculated from layout considerations of the memory, assuming about  $600\lambda^2$  per memory cell.  $C_{diff}$  is the diffusion capacitance of one memory transistor.

The power dissipated is calculated assuming one instruction per cycle, and the fact that approximately 30% of all data instructions are memory operations, resulting in 1.3 memory instructions per cycle ??.

#### D. Leakage power dissipation model

For the leakage power calculation, total leakage current is calculated based on the ITRS projections for transistor leakage current per unit width. The expression for the static leakage power is given by

$$P_{leakage} = W_{avg} I_{leak} N_{trans} V_{dd}$$

Where  $I_{leak}$  is the leakage current per unit width, and  $W_{avg}$  is as defined above.  $N_{trans}$  is the total number of transistors, taken separately for logic and memory.

#### E. Clock power dissipation model

Depending on skew objectives, there are a number of clock distribution schemes. The least expensive in terms of power, but with most skew, is the H-tree based clock distribution scheme. Most aggressive is a complete grid based clock distribution of the Alpha microprocessors that achieves low skews even with non-uniform loading ?. We consider an H-tree based distribution for the global clock is then followed by a grid based distribution for the local clock. A schematic for this clock distribution scheme is shown in Figure 1.

The global clock distribution capacitance has two components: the wiring capacitance for the global H-tree, and the capacitance of the clock tree buffers. The wiring capacitance of

the H-tree network is derived to be

$$C_{H-tree} = 3L_c C_w \left(1 - \left(\frac{1}{2}\right)^k\right)$$

$L_c$  is the edge-length of logic area, and  $C_w$  is the capacitance per unit length for the global wire.  $k$  depends on the number of spine location to be driven by the H-tree and is given as

$$k = \log_2(N_{spine}) - 1$$

In this case,  $N_{spine}$ , the number of spine locations, is the same as the number of isochronous regions.

The buffer capacitance for the H-tree depends on the final load, which is the capacitance of the grid and the latches. For a width ratio of 4, for optimum delay ??, the buffer capacitance for the H-tree is given by

$$C_{buf} = (C_{grid} + C_{latch}) \sum_{n=0}^{N_{stage}} \left(\frac{1}{4}\right)^n \approx 0.33(C_{grid} + C_{latch})$$

The total power dissipation in the global clock distribution is

$$P_{clock,global} = (C_{H-tree} + C_{buf}) V_{dd}^2 f_{global}$$

In a typical design, for a desired clock skew, grid dimensions are dictated by the non-uniformity of the load. However, it has been observed that a typical grid wiring density of 3-6% of one entire intermediate wiring layer achieves the desired skew ?. We compute the grid wiring area based on a round figure of 5%. Grid pitch is assumed to be the intermediate wiring pitch. The latch capacitance is calculated as

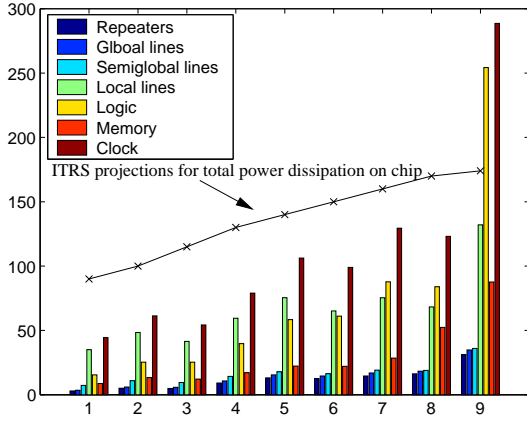
$$C_{latch} = \left(\frac{1}{f_{ld}}\right) W_{avg} N_{logic} C_{trans}$$

The formulation is similar to the one used for power dissipation in logic. The total clock distribution power is evaluated as

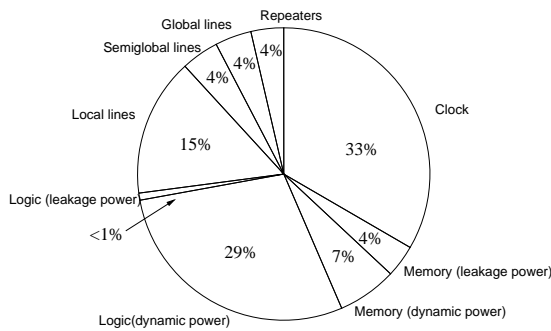
$$P_{clock} = P_{clock,global} + P_{grid} + P_{latch}$$

## 4. RESULTS AND DISCUSSION

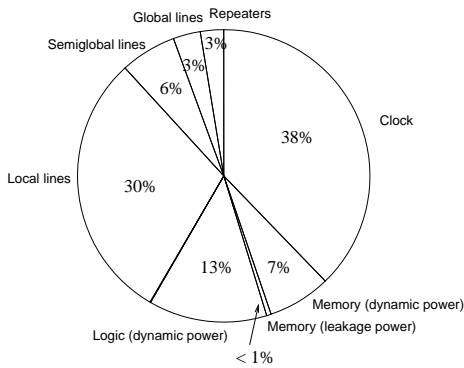
Figure 2 shows the histogram of the various power components at future technology nodes. ITRS projections for the total chip budget is also plotted for reference. It is seen that clock distribution alone runs into more than 250W at the 50nm technology node, and is likely to be the most serious problem unless innovative schemes are applied. The power dissipation in logic gates alone also exceeds the ITRS chip budget. Other components, though overshadowed by above two, are also getting larger. To get an idea of how the components scale in terms of their fractional contribution, we plot the breakdown of power at the 50nm technology node in Figure 3. Figure 4 shows the breakdown at the present technology node, for comparison.



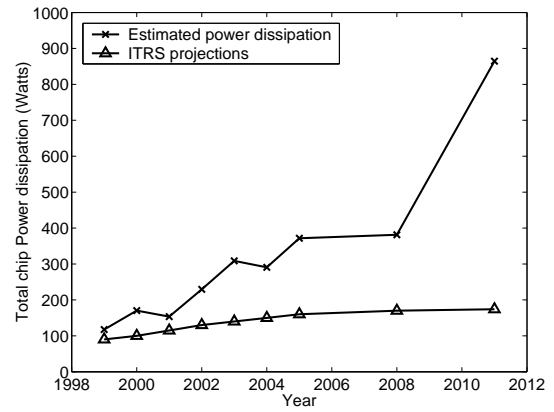
**Fig. 2.** Scaling of various power components in the future



**Fig. 3.** Breakdown of power in year 2011 (50nm technology node)



**Fig. 4.** Breakdown of power at the present technology node



**Fig. 5.** Estimation of total chip power, and comparison with ITRS projections

It is seen that the percentage of dynamic power dissipated in the logic increases, at the cost of interconnect power going down. Most other components do not change significantly. However, it might be wrong to infer that interconnects would not be a problem, since in absolute numbers the interconnect power dissipation also increases significantly.

Figure 5 plots the total power dissipation, comparing with the ITRS projections. The estimated power dissipation soon grows to exorbitant proportions. Thus, unless the design methodologies undergo lots of changes, power dissipation is likely to be a very serious problem, reaching unmanageable limits.

## 5. CONCLUSION

A complete model for the on-chip power dissipation is presented, followed by the analysis of scaling of various components of power. It is seen that clock distribution and dynamic power dissipation in the logic are the two most important entities, though the power dissipation of other components is, by no means, small. As a result, the total power dissipation of the chip would far exceed the ITRS projections unless innovative design methodologies are adapted.

- [1] International Technology Roadmap for Semiconductors, 1999
- [2] Davis et al, A stochastic wirelength distribution for GSI Integration, blah blah
- [3] BACPAC
- [4] Computer Architecture: A Quantitative Approach, Hennessy and Patterson
- [5] Bailey et al, Clocking Design and Analysis for a 600MHz Alpha Microprocessor, IEEE JSSC, Nov. 1998
- [6] Liu et al, Power Consumption Estimation in CMOS VLSI Chips, IEEE JSSC, June 1994