

Impact of Joule Heating on Deep Sub-Micron Cu/low-k Interconnects

Ting-Yen Chiang, Ben Shieh and Krishna C. Saraswat

Department of Electrical Engineering, Stanford University, Stanford, CA 94305
{tychiang, bshieh, saraswat}@stanford.edu

Abstract

This paper investigates the impact of Joule heating on the scaling trends of advanced VLSI interconnects. It shows that the interconnect Joule heating can strongly affect the maximum operating temperature of the global wires which, in turn, will constrain the scaling of current density to mitigate electromigration and, thus, greatly degrade the expected speed improvement from the use of low-k dielectrics. Through a combination of extensive electrothermal simulation and 2D field solver for capacitance calculation, the thermal characteristics of various Cu/low-k schemes are quantified and their effects on electromigration reliability and interconnect delay is determined. The effect of vias, as efficient heat conduction paths, is included for realistic evaluation. Our analysis suggests that the Joule heating will be a bottleneck in scaling interconnects and will not meet the projection of International Technology Roadmap for Semiconductors (ITRS'01) [1] requirements.

I. Introduction

As VLSI technology advances, interconnects have become the limiting factor to IC chip performance [2]. Aggressive interconnect scaling has resulted in increasing current density, more metal levels, and introduction of low dielectric constant (low-k) materials. However, due to the poor thermal properties of inter layer dielectrics (ILD), as shown in Fig.1, Joule heating of the interconnect wires is fast emerging as an urgent issue. The work presented here is for the 65nm technology node with all parameters quoted from the newly updated ITRS '01. We assign first two metal layers as local tier, the following four layers as semi-global tier and the remaining layers as global tier. The substrate temperature, T_{ref} , is assumed to be fixed at 100°C (which will be true if two-phase microchannel cooler is employed in the future [3]), and the temperature of the top global wire is $T_m = T_{ref} + T_{joule\ heating}$.

II. Definition of Worst Case Condition

To provide robust thermal analysis for interconnects, it is important to identify a reasonable worst case scenario. Previous work has attempted to evaluate the thermal characteristics of interconnects neglecting vias as an effective heat conduction path [4]. However, ignoring vias in heat transfer predicts unrealistically high temperature rises even with moderate current densities. This is especially true for dielectrics with lower thermal conductivities [5,6]. Therefore, this paper will include the via effect in the analysis to obtain more realistic results. Case(1) in Fig. 2 shows the widely used condition, i.e., all wires flowing the same current density and the via effect ignored. Case(2) represents an isolated global wire. Although there is no additional heat sources between this wire and the substrate, the thermal impedance is higher in the absence of lower level metal. Case(3) has the same current condition as case(1) but with vias taken into account for all metal layers. Reasonable via separations are assigned for each metal level from level one to ten: 5, 20, 50, 100, 150, 200, 300, 500, 1000 and 2500. As shown in Fig. 3, case(1) has the highest temperature rise. But we will disregard this condition as unrealistic as vias are ignored. Case(3) is worse than case(2) and we will use this condition for the following analysis.

III. Temperature Effect on Cu/low-k Interconnects

Fig.4. shows the thermal performance of several low-k materials. As the figure shows, interconnects with lower dielectric constant materials exhibit significantly higher temperature rises. The product of $R_{met}C_{total}$ per unit length for these dielectrics is shown in Fig. 5 as a function of current density. As the figure shows, the low-K advantage of reduced capacitance can be offset by the increased temperature rise due to poor thermal conductivity. It should be noted that for the case of air-gap scheme (ILD: SiO₂ and IMD: Air), the $R_{met}C_{total}$ is relatively constant through the range of current density and it is even better than polyimide. This is because air-gaps reduce the dominating line-to-line capacitance while leaving the SiO₂ ILD intact for better thermal conductivity. Since

electromigration mean time to failure (MTF) is exponentially dependent on wire temperature, the maximum allowable current density for a given temperature rise is evaluated in Fig. 6 for different low-K materials.

IV. Delay and Reliability Optimization

With the possibility that much fatter wires may be used in the global tier to reduce IR drop, it is important to know the thermal impact of using low aspect ratio lines on the expected performance and reliability. In addition, ILD thickness should be evaluated to assess the trade-offs of thermal impedance and capacitance. The contours of constant $R_{met}C_{total}$, in Fig.7 show the optimization of the wire aspect ratio (AR) and the ILD thickness for delay consideration. It demonstrates that Joule heating can increase delay of the interconnect by as much as 15%. Fig. 8 shows constant MTF contours, with the temperature effect included. The MTF can never reach 50% of MTF at 105°C which is the wire temperature specified in ITRS. We can conclude from Fig. 7 and 8 that although fat wires can provide better speed performance, but they are also more subject to electromigration failure since the temperature is higher.

V. Impact of Joule Heating on Scaling Trend

Table 1 shows the coupled analysis of delay and electromigration MTF for various technology nodes. Column 2 shows the maximum current density specified in ITRS and column 3 shows the resultant temperature of the top global wires. The $R_{met}C_{total}$ delay is shown in column 4 and the corresponding MTF is shown in Fig. 9 as the solid curve. The achievable MTF is about 90% at 130nm node, but drops sharply for the following technology nodes. The $MTF(T_m)$ is compared to the $MTF(105^\circ C)$. To confine the wire temperature at 105°C, the current density has to be reduced as shown in column 4 and resultant current drive, compared to the maximum current density specified in ITRS, drops drastically as can be observed in column 5. To relax the temperature rise to 10°C above substrate, the current drive can be improved as shown column 7. We notice that in both cases trying to match certain specific wire temperatures (105°C and 110°C), the corresponding MTF rises above the required MTF, as shown in Fig.9. It implies that this approach is overly conservative. Since the MTF of electromigration is also inversely proportional to the square of current density, as modeled by the well-known Black equation, we can achieve the expected MTF by optimizing both the current density and wire temperature, which are related by Joule heating. The result is shown in the last three columns of the table. The optimal current density is much closer to the value specified in ITRS. On the other hand, although the wire temperature is higher than 105°C, as shown in the last column, the MTF is on target, as shown in the flat line in Fig.9.

VI. Summary

In conclusion, a detailed analysis of the impact of Joule heating on the characteristics of future Cu/low-k interconnects is presented using a realistic full chip model with via effect included. Thermal effect can severely degrade both reliability and speed performance. Optimization with various interconnect parameters is provided. Joule heating will limit scaling of current density and use of low-k materials. Global wires will be more problematic with higher operating temperature and careful consideration is imperative.

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References

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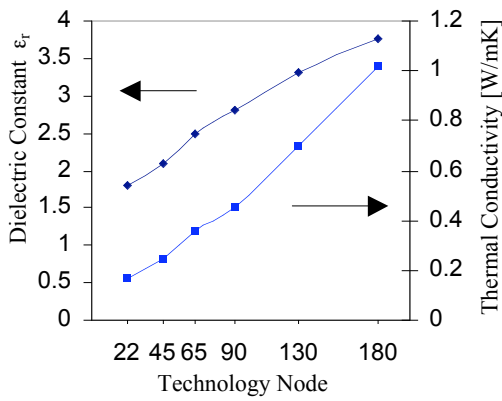


Fig. 1. Both dielectric constant and thermal conductivity of dielectrics decrease for advanced technology nodes.

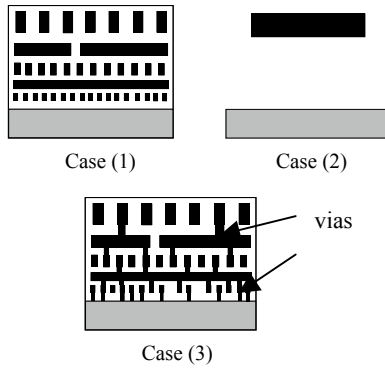


Fig. 2. Configurations of the three thermally worst case scenarios. Current flows through all wires at all metal layers in cases (1) and (3).

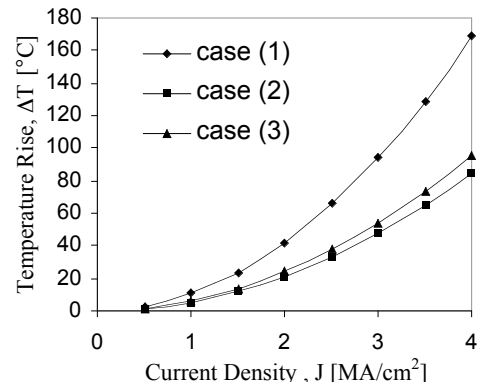


Fig. 3. Temperature rise comparison of the three thermally worst case scenarios. To simulate the more realistic condition, cases (3) is chosen over case (1) for the rest of the thermal analysis in this paper.

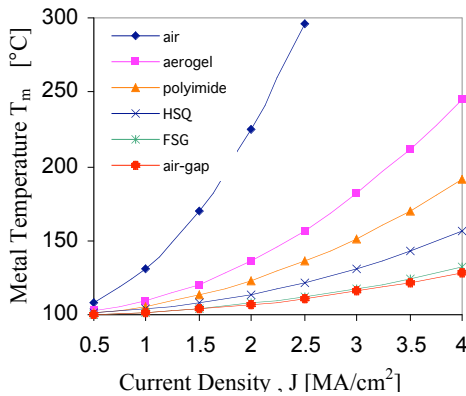


Fig. 4. Temperature of top global interconnects rises sharply for Low-k dielectrics. Interconnect dimensions are taken from the 65nm technology node from ITRS.

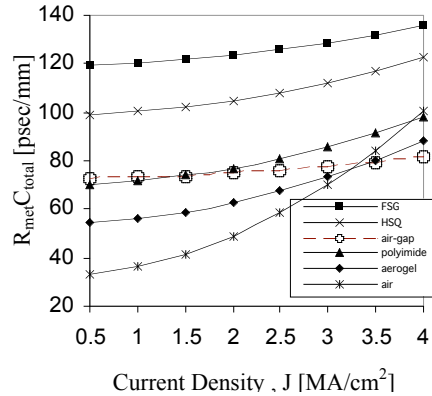


Fig. 5. RC delay is strong function of current density on the wires because of Joule heating. The lower the dielectric constant, the stronger the Joule heating and greater RC degradation.

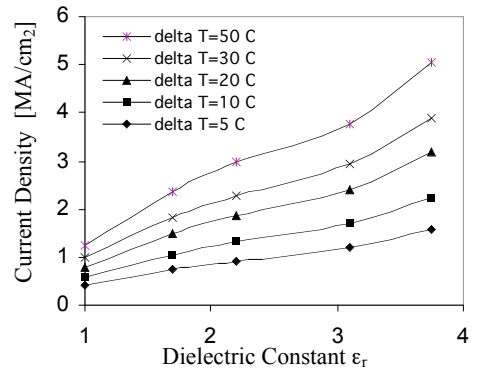


Fig. 6. Maximum allowed current density is limited by the maximum allowed ΔT on the metal wires. The constraint is more stringent for low-k dielectrics.

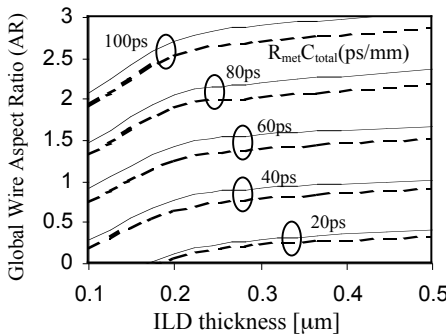


Fig. 7. Constant $R_{met}C_{total}$ contour plots of global level wiring as functions of wire aspect ratio (AR) and ILD thickness. Solid curves represent the case thermal effect neglected. Dash-line curves include the influence of thermal effect. (H/S=0.32/0.15 μm)

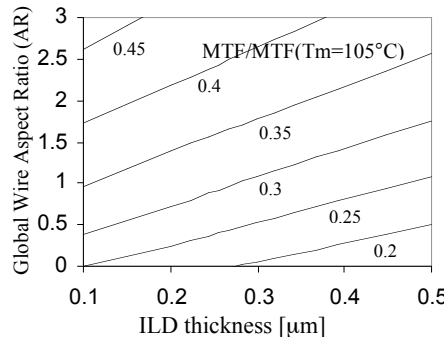


Fig. 8. Constant normalized electromigration MTF, $MTF(T_m)/MTF(105^\circ C)$, contour plots of global level wiring as functions of wire aspect ratio (AR) and ILD thickness. (H/S=0.32/0.15 μm)

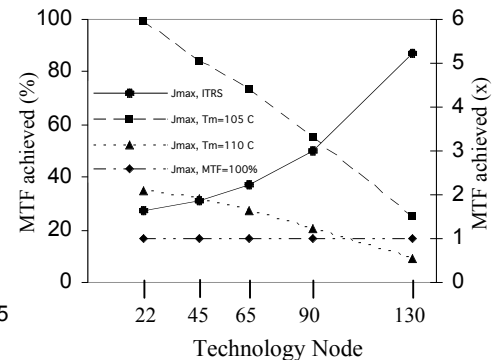


Fig. 9. The solid curve shows the MTF (%) that can be achieved under the current density specified in ITRS. The broken-line curves show the MTF under various wire temperature (T_m) criteria and the values refer to the right axis..

Tech. Node	Max. J_{rms} (ITRS) [MA/cm ²]	T_m [°C]	$R_{met}C_{total}(T_m)$ normalized to $R_{met}C_{total}(T_m=105^\circ C)$	J_{rms} $T_m=105^\circ C$ [MA/cm ²]	Current drivability normalized to Max. J_{rms}	J_{rms} $T_m=110^\circ C$ [MA/cm ²]	Current drivability normalized to Max. J_{rms}	$J_{rms,optimal}$ MTF=MTF($T_m=105^\circ C$) [MA/cm ²]	Current drivability normalized to Max. J_{rms}	T_m [°C]
130	0.96	107	1.01	0.79	0.82	1.12	1.16	0.91	0.95	106
90	1.5	117	1.05	0.82	0.55	1.16	0.78	1.24	0.83	111
65	2.1	122	1.09	1.0	0.48	1.41	0.67	1.64	0.78	113
45	2.7	126	1.09	1.2	0.44	1.69	0.63	2.04	0.76	114
22	3.9	128	1.10	1.6	0.41	2.33	0.60	2.84	0.73	116

Table 1. Coupled evaluation of electromigration reliability and performance for global interconnects for 22-130 nm technology nodes. T_m is the top global wire temperature with all the heat sources, including substrate and Joule heating from all metal levels underneath, taken into account.