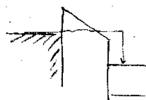
EE 311 Spring 1999
Solution to the Midterm Exam

1. In an MOS transistor a 3 nm thick gate SiO_2 is replaced by a 30 nm thick hypothetical dielectric with same band gap as that of SiO_2 but 10 times its K. Under constant current gate injection which transistor will give lower Q_{bd}? Assume same energy is required to create damage in both materials.

* SiO_2 : 3nm, K high k : 30nm, 10k

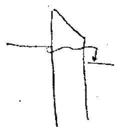
=> electrical length is same in both cases.



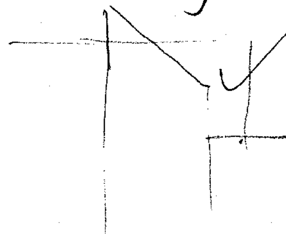
Q_{BD} depends on : 1. Thickness of dielectric
2. Interface structure
3, 4 : Temp, J_{stress}

#1, 2 are different in the 2 cases.

@ 3nm, we will have lots of tunneling current, which implies lower energy available for breaking bonds.



Since current is maintained const, we will need to apply a much higher voltage for high-k material (∵ It's mostly not going to be in the tunneling regime) So, lots of energy will be available for breaking bonds in high k.



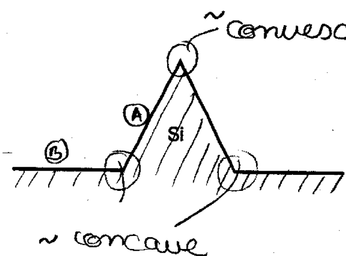
Also, the interface (Si - dielectric) is likely to be worse in high-k as compared to SiO_2.

Both these factors imply

$$Q_{BD}\big|_{SiO_2} > Q_{BD}\big|_{high\,k}$$

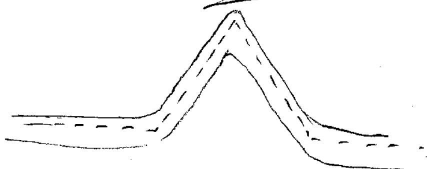
2. Thermal oxidation of a pointed Si wedge shown below is done. Sketch the shape of the grown oxide and remaining Si as a function of
    a) oxidation time - short and long
    b) oxidation temperature - low and high

a) oxidation time - short and long
b) oxidation temperature - low and high



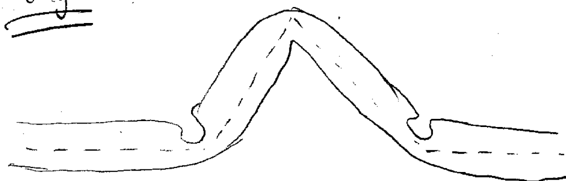
NOTE: The edge (A) will have a different crystal orientation than edge (B) and hence oxidation rates will be diff. But I am ignoring it here

a. Time : Short :



This oxide (due to shorter time) does NOT show any prominent 2-D osc effects & hence almost conformal oxide is obtained.

long

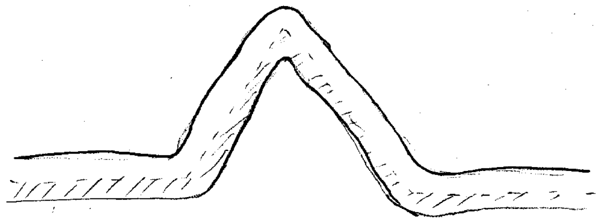


for long osc., a pronounced 2D oxidation effect is observed.

--- : original Si interface

b.

low T



high T

The 2D effects are more pronounced @ low T's
we see a near air gap @ concave point & thinner oxide on convex point @ lower T
Reason: high T's, less viscosity, can flow well

3. Trench isolation is used for a CMOS product. The trench is filled in one case with solid SiO_2 and in the other case with a porous dielectric with lots of microvoids but with an ultrathin layer of SiO_2 at the trench surface as shown in the figure below. Which structure will give lower transistor leakage realizing that the transistor fabrication will require several thermal cycles?

* The Porous dielectric gives Lower Leakage.

Reasons: Tce mismatches

* And further oxide growth in the Trench can cause Compressive stress in the Silicon.

* This stress causes increased Leakage current in the Si.

* SiO_2 filled trench is likely to exert more pressure on the surrounding Silicon (it is more solid and does not compress)

* The Porous dielectric is more likely to Compress, releiving the Stress on the Silicon.
  ⇒ Lower Leakage Current.

4. The figure below shows an ideal and a realistic PtSi contact to Si doped with arsenic to the solid solubility limit. The latter case results due to Si consumption. Which structure will give lower contact resistance if we assume that dopant segregates into Si during the silicide formation?

If we assume that the dopant segregate into the Si during the silicide formation, i.e. there is no dopant loss to the silicide then the contact area for b is larger & so it will give a lower contact resistance.

(note: the above answer is true assuming that there is no dopant pile up at either of the interfaces which could lead to dopant deactivation. This cannot be taken into accounts as the model for dopant pile up in (a) is not known)

If there is no dopant segregation then a lot of the dopant is lost to the silicide which drains them away very quickly (as dopants diffuse very quickly thru silicides) & so the dopant concentration in silicon becomes very low & we get a schottky barrier. With dopant segregation (again assuming no dopant deactivation) an ohmic contact is maintained & so the ρ_c is low