

EE282H Homework #1

Due Tue October 6, 1998

Question 1.0

Exercise 1.2 from H&P text

Question 2.0

A silicon valley company is looking into ways to increase the performance of its workstations. Analysis of the applications that its customers are using has shown that average response time breaks down into three main categories: CPU time, memory system time and host/client communications time.

A meeting is convened to discuss how the response time can be improved. At the meeting, the network people are quite embarrassed by the proportion of host/client communications time, and they promise that by using a more suitable network, host/client communications will be sped up by 10 times.

Next, the memory system designers speak, and they predict that by using a new design the memory system time can be reduced to 10% of the total response time. (Assuming that the other two components are not changed.)

2.a If after only the network changes, the response time is distributed 74%, 25% and 1% between the CPU, memory system and communications respectively, how much faster are the original workstations after both the network and memory system improvements

Lastly, the CPU designers take the podium, and they announce (having listened carefully to the previous two groups) that including their enhancements to the CPU, the total speedup (after all three groups's improvements) will be 2 times.

2.b How much are the CPU designers planning to speedup the CPU?

Question 3.0

The base DLX implementation (you will become quite familiar with this ISA by the end of the course, but you don't need to know anything about DLX to answer this question) does not have a FP coprocessor and must emulate all floating point instructions in software. Your team has the task of developing a DLX-FP machine with a FP coprocessor. The current DLX machine runs at 25Mhz, and your new DLX-FP machine is expected to run at 50MHZ.

To evaluate the performance of your DLX-FP machine, you will use the Flintstone benchmark. For this benchmark you measure the following data.

Instruction type	DLX CPI	DLX-FP CPI	DLX-FP Instruction Count
Branches/Jumps	1.3	1.3	775,000
Integer ALU	1.3	1.3	380,000
Load/Store	1.3	1.6	975,000
Floating Point	N/A	15.0	1,750,000

3.a The current DLX machine without the FP coprocessor takes 5 seconds to run the benchmark. How many seconds does it spend emulating floating point instructions?

3.b On average, how many integer instructions does it take to emulate each floating point instruction?

3.c Because of the increase in die area and the more aggressive technology, the DLX-FP microprocessor is expected to cost 10 times more than the current machine. Your boss wants the new machine to have at least the same cost/performance as the original machine. What must the average CPI of the DLX-FP floating point instructions be reduced to in order to have the same cost performance as the current DLX machine? Assume that the CPI of all non-floating point instructions are unchanged.

Question 4.0

Exercise 1.15 from H&P text.