

## Quiz: Are you in the right class? EE282H Computer Architecture

This quiz is to take home and review on your own. You should be able to answer the following questions easily.

1. Define the following terms:

- a. multiplexor
- b. full adder and half adder
- c. paging
- d. segmentation
- e. ALU

2. Write the code sequence for the following code for the different style machines listed below:

```
while x<z do x:=x+y;
```

- a. a stack machine
  - b. a machine with powerful addressing modes and general purpose registers.
3. Draw a block level diagram of a machine with 16 registers, 32-bit instructions, and 3-register ALU operations, and a single address mode (for loads and stores) that adds a displacement in the instruction to a register contents to get a memory address. List the execution steps (what happens on each clock) for the following two instructions:

```
ADD R1,R2,R3
```

```
LOAD R4,42(R5)
```

4. How do the cache parameters block size and set-associativity affect the miss rate of the cache as they are varied over a wide range?
5. Why is miss rate a misleading indicator of cache performance?

**If you cannot do these problems easily, you should take EE182.**