

b) [20 points] After cycle 7, they think that their simulator may have made some mistakes. Find 2 errors in the pipeline diagram during the later cycles, note any corrections on the diagram, and explain why you made the corrections. Note that a single “error” may have been propagated through several different instructions — these still count as a single error, however, for the purposes of this problem. Instead, you should look for conceptually different errors.

Error #1 Explanation:

Error #2 Explanation:

c) [5 points] The engineers also ask you to address the performance of their machine. Why does the second iteration of the loop take so much longer than the first to issue? What simple hardware change could be made to eliminate this problem?

d) [5 points] Even with your suggestions to improve the second iteration’s performance, their processor is still only issuing $12/7 = 1.71$ instructions per cycle, far below their target of 4 per cycle. They ask you for a suggestion to economically make their processor run closer to its specified target.

e) [5 points] In what types of places would a scoreboard version of this processor be forced to stall, where this Tomasulo’s version was allowed to continue processing? Note a specific example from the pipeline that illustrates a possible stall in a scoreboard version of the processor.

f) [5 points] Why should stores be performed by the reorder buffer instead of an execution unit?