

ISA Design Homework

Due October 15, 1997

Question 1 (30 points)

2.1 from textbook.

Question 2 (20 points)

2.3 from textbook.

Question 3 (20 points)

2.6 from textbook. Instead of writing code answer question for code on slides 23 and 23 of the Lecture 3 notes.

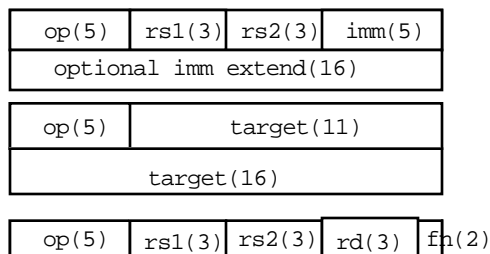
Question 4 (15 points)

2.11 from textbook.

Question 5 (40 points)

You have been asked to evaluate a version of the DLX ISA called DLX-short. DLX-short has instructions that are 16-bits or 32-bits long. DLX-short is intended for the embedded CPU core market where it is critical to keep memory usage and memory bandwidth requirements low. The DLX-short ISA has no support for floating point instructions. The instruction formats for DLX-short are shown below (the encodings are shown below the table)

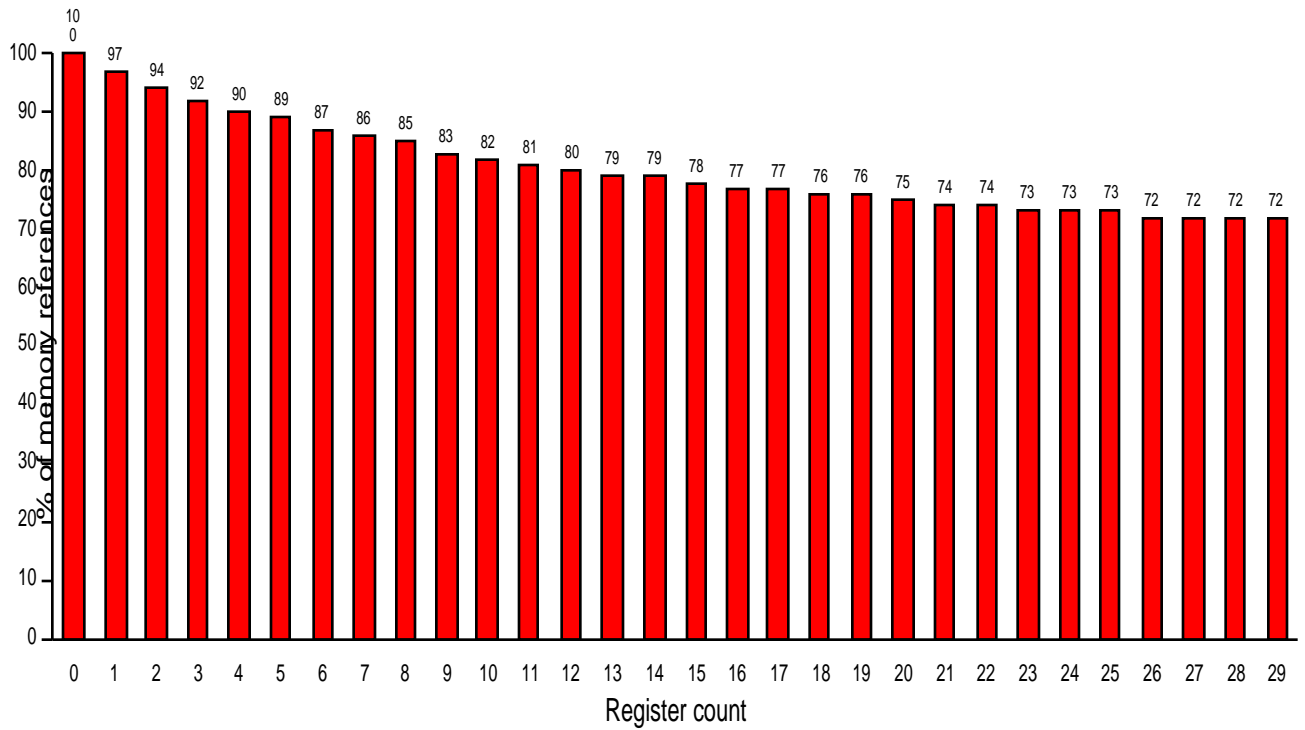
Format	Encoding	Instructions
I-type		loads & stores conditional branches all ALU immediates jump register imm extend is only used by the compiler if needed
J-type		jump jump & link
R-type		all register-register ALU instructions



Assume the following about DLX and DLX-short

- 32-bit wide registers
- $r0 = 0$
- The compiler claims two registers for the stack pointer (sp) and global pointer (gp).

To evaluate this architecture you collect the following data on the DLX ISA



#Immediate bits for magnitude	Cumulative Immediates (%)
0	0
4	60
8	80
12	90
15	100

Table 1: Number of bits needed for magnitude of immediate value in DLX immediate field.

Offset bits/	Cumulative data references (%)	Cumulative branches (%)
0	17	0
1	17	0
2	23	24
3	32	49
4	40	64
5	48	79
6	54	87
7	57	93
8	60	98
9	61	99
10	69	100
11	71	100
12	75	100
13	78	100
14	80	100
15	100	100

Table 2: Cumulative percentage of data references and branches with number of bits of magnitude that can be accommodated in the displacement (sign-bit is not included).

Instruction	Frequency (%)
load/store	37
ALU imm	25
ALU reg-reg	15
load imm.	7
branch	13
call	1.5
return	1.5

Table 3: DLX instruction mix

2.a (10 points)

What is the instruction mix for the DLX-short ISA?

2.b (10 points)

What are the ratios of instruction count and data memory accesses for the two architectures (DLX-short/DLX).

2.c (15 points)

What is the ratio instruction bytes fetched for the two architectures (DLX-short/DLX).

2.d (5 points)

What is the ratio of bytes that cross the CPU/memory boundary for the two architectures (DLX-short/DLX).