
Tapeout Checks

EE272 Winter 2003

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Tapeout checks

Why do them?

- Make sure what you send to fab is what you want
- Must be done on top-level layout (including pads)
 - Good to run checks on lower level hierarchy first
- Assumes you've already done DRC and LVS checks

What are they?

- Clean CIF/calma generation
- Routing through labels
- Floating wells
- Routing through wells
- Layout versus layout (LVL)

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Clean CIF/calma generation

- Calma generation (makes a .strm file)
:calma
- Parent child disagreements must be fixed
 - Duplicate layout
 - Remove duplicate contact on one side
 - Flatten the cells
- Interacting CIF warning
 - Flatten the cells into larger blocks
- Splinter warnings
 - Ignore
 - Any problems should be caught in later checks (LVL)

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Routing through labels

Make sure that there are no virtual node connections

- Extract your magic layout
- Have NO extraction warnings in any level of hierarchy
 - If you do, use :feed find to find them
- You could also strip out all labels from your layout then run gemini against your schematics

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Floating N wells

Make sure that all nwells are connected to Vdd

- Start a fresh Magic session
- Extract using check_nwell style
 - :ext style check_nwell
 - :ext all
- Run ext2sim
- Look at the .sim file
 - You should only have caps between Vdd and Gnd
 - If you have other caps, these are the floating well nodes
 - Find these floating wells and put in a well contact!

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Floating P wells

Make sure that no node is shorted to the substrate

- Start a fresh Magic session
- Extract using the check_pwell style
 - :ext style check_pwell
 - :ext all
- Run ext2sim
- Look at the .sim file
 - There should only be a Gnd to Gnd cap
 - Any other cap node is a node shorted to the substrate
 - Find these nodes and remove the erroneous substrate contact!

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Routing through wells

Make sure that Vdd is not routed through Nwells

- Make a copy of your normal top-level .sim file
- Run magic with the special well-route techfile
Magic -T ee272_05_WR chip
- Extract your layout again
:ext all
- Run ext2sim to create a new top-level .sim
- Use gemini to compare the two .sim files
 - They should match
 - If not, then use the gemini output to find where you routed Vdd through a Nwell

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Layout versus layout

Make sure that the calma output is correct

- Generate the calma output as normal
- Move the .strm file to a new directory
- Start Magic, and do
:calma read chip
:load chip
:ext all
- Run ext2sim on the new extraction
- Run gemini between the new .sim and the normal .sim
 - They should match

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