EE183 Fact Sheet

What is EE183?

EE183 is a largely hands-on lab class, which emphasizes independent work. You will be designing digital circuits and then implementing your designs using modern programmable logic devices.

There is no set lab meeting time – you have 24-hour access to the facilities and may work at any time.

What is required?

You must complete four lab projects. A written report is required with every lab in addition to the demonstration of the project to the TA or instructor. There will be one exam during the quarter covering the lectures and the lab material. All your work must be finished by **Monday, March 17**. **NO INCOMPLETES** will be given.

Class Time: MW 8:00-8:50 a.m. (a few Fridays, see schedule below)

Lecture Room: Gates B12.

EE183 Lab: Packard 129
725-1767

Instructor: Kunle Olukotun
Kunle@stanford.edu
Office hours MW 9-10 am in Gates 302 and Packard 129

TA: David Black-Schaffer
davidbbs@stanford.edu
Office Hours TBD in Packard 129

Course Secretary: Darlene Hadding
Gates 408
650-723-1430
darlene@mojave.stanford.edu

Office Hours: Hours are subject to change and will be posted on the web. Please check the web page periodically for announcements and changes to the office hours.

Exam: There will be a 2-hour exam given in February.

Prerequisites: EE121 and EE182 (EE182 may be taken concurrently)

Required Text: There is no required text.

Recommended: Wakerly, Digital Design Principles and Practices (textbook from EE121).

Building Access: Your SUID will give you access to the Packard building and rooms 129 (lab) and 128 (computer room). Please see David for details.

Grading: Projects account for 80% of the final grade and the exam makes up the remaining 20%. For the projects, 50% of the score is for demonstrating the working circuit (**no non-working circuits will be accepted**) and 50% is for the project report. The labs are worth 40 points each (i.e., 20 points for the demonstration and 20 points for the write-

up). The final project is worth 60 points (20 additional points for innovation and complexity). Class participation and lab usage can also influence the final grade.

Late Penalty: It is very important to stay on track with this course. There will be no free late days or extensions given. The late penalty, both for demos and writeups, is 2 points per calendar day late. Labs must be completed, even for 0 points, to finish the course.

Lecture Schedule: The lecture schedule has not been finalized, but the following is a tentative schedule of dates and topics. Everyone is expected to come to all the lectures.

Wednesday, January 8 Friday, January 10	Introduction/Design Flow
Monday, January 13 Wednesday, January 15	
Wednesday, January 22 Friday, January 24	
Monday, January 27 Wednesday, January 29	
Monday, February 3 Wednesday, February 5	
Monday, February 10 Wednesday, February 12	
Wednesday, February 26	**Exam, 7-9 p.m.**
Friday, March 14	**Bagle Day, project disc., class eval.,**

Lab Schedule: Pre-lab write-ups are due a week before the demonstration.
Final write-ups are due the next weekday.

Lab	Pre-Lab Write-Up Due	Demo Due by 5 p.m.	Final Write-Up Due
1st Lab	January 17	January 24	January 27
2nd Lab	January 30	February 7	February 10
3rd Lab	February 14	February 21	February 24
4th Lab	February 28	March 7	March 10