EE183 Course Overview

What is EE183?

EE183 is a largely hands-on lab class, which emphasizes independent work. You will be designing digital circuits and then implementing your designs using modern programmable logic devices. The emphasis of this course is in getting you to do digital system design, so the specifications for the lab assignments may seem somewhat broad at first.

There is no set lab meeting time – you have 24-hour access to the facilities and may work at any time.

What is required?

You must complete four lab projects. A written report is required with every lab in addition to the demonstration of the project to the TA or instructor. There will be one exam during the quarter covering the lectures and the lab material. All your work must be finished by the last day of classes, **Wednesday, June 4**. **NO INCOMPLETES** will be given.

Class Time: MW 8:00-8:50 a.m. (a few Fridays, see schedule below)

Lecture Room: Teaching Center in the Science and Engineering Quad (TCSeQ) Room 101.

EE183 Lab: Packard 129
725-1767

Instructor: David Black-Schaffer
davidbbs@stanford.edu
Office Hours: 10am-11am Mon, Wed, Fri and Fridays 3-5pm when labs are due.

TA: Joel Coburn
jcoburn@stanford.edu
Office Hours: TBD

Course Secretary: Darlene Hadding
Gates 408
650-723-1430
darlene@mojave.stanford.edu

Office Hours: Hours are subject to change and will be posted on the web. Please check the web page periodically for announcements and changes to the office hours.

Exam: There will be a 2-hour exam given on the 14th of May.

Prerequisites: EE121 and EE182 (EE182 may be taken concurrently)

Required Text: There is no required text.

Recommended: Wakerly, Digital Design Principles and Practices (textbook from EE121).

Building Access: Your SUID will give you access to the Packard building and rooms 129 (lab) and 128 (computer room). Please see Paul or David for details.

Grading: Projects account for 80% of the final grade and the exam and final project difficulty make up the remaining 20%. For the projects, 50% of the score is for demonstrating the working circuit (**no non-working demos will be accepted**) and 50% is for the project report. The labs are

worth 40 points each (i.e., 20 points for the demonstration and 20 points for the write-up). Pre-labs are worth 10% of each write-up. Points will also be deducted for late write-ups and pre-labs. Details on the write-up and pre-lab formats are on the course webpage. The final project is worth 60 points (20 additional points for innovation and complexity). Class participation and lab usage can also influence the final grade. The exam will be open notes and should be straight forward if you attended the lectures.

Late Penalty: It is very important to stay on track with this course. There will be no free late days or extensions given. The late penalty, both for demos and write-ups, is 2 points per calendar day late. Labs must be completed, even for 0 points, to finish the course.

Lecture Schedule: The lecture schedule has not been finalized, but the following is a tentative schedule of dates and topics. Everyone is expected to come to all the lectures as the labs themselves will be explained in detail in the lectures.

Wednesday, April 2	Introduction & FSM Review
Friday, April 4	Verilog
Monday, April 7	VGA and the Game of Life
Wednesday, April 9	Lab 1 and Timing
Monday, April 14	More on Timing
Wednesday, April 16	Documentation and Controller Design
Monday, April 21	Fractals
Wednesday, April 23	Performance
Monday, April 28	**Guest Lecture** - Metastability/Synchronization
Wednesday, April 30	Microprocessors
Monday, May 5	Microprocessors
Wednesday, May 7	Communication Methods/Guest Lecture?
Monday, May 12	Final Project
Wednesday, May 14	**Exam, 7-9 p.m.**

Lab Schedule: Pre-lab write-ups are due a week before the demonstration.
Final write-ups are due by midnight the Monday after the labs are due, or 24 hours after you demo if you are late.

Lab	Pre-Lab Write-Up Due by 5 p.m.	Demo Due by 5 p.m.	Final Write-Up Due by midnight
Tutorial	none	none	Wed. April 9 (short write-up)
1st Lab	Fri. April 11	Fri. April 18	Mon. April 21
2nd Lab	Fri. April 25	Fri. May 2	Mon. May 5
3rd Lab	Fri. May 9	Fri. May 16	Mon. May 19
4th Lab	Wed. May 21	Mon. June 2	Wed. June 4