CS140 Operating Systems and Systems Programming
Midterm Exam

October 24, 2008

(Total time = 50 minutes, Total Points = 50)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

This examination is close notes and close book. You may not collaborate in any manner on this exam. You have 50 minutes to complete the exam. Before starting, please check to make sure that you have all 9 pages.

1	
2	
3	
4	
5	
6	
7	
Total	

1. (12 points) For each of the changes described below, state the effect on the following hardware-defined data structure: the Page Table, a Page Table Entry (PTE), and the TLB. For each data structure, describe if it will increase in size, decrease in size, or stay the same size. Be sure to justify your answer.

a) Increasing the number of virtual address bits in the architecture.
Page Table:

Page Table Entry:

TLB:

b) Increasing the number of physical address bits in the architecture.
Page Table:

Page Table Entry:

TLB:

Question 1) continued….

c) Increasing the number of processes/address spaces that can be active in the MMU at a time.
Page Table:

Page Table Entry:

TLB:

2. (6 points) Assume you are given a modern OS environment that switches from using only statically linked object files to using shared dynamically linked libraries (DLLs) for all applications. For each of the following counts, describe if you would expect the count to increase, decrease, or stay the same.

   a) Number of code pages read from disk.

   b) Number of code pages in virtual memory across all the processes.

   c) Number of TLB misses an application suffers

3. (5 points) Describe an algorithm that computes the **Idle Time** of a page that is needed for the **Working Set** algorithm.

4. (5 points) Explain the mechanism used by VMS and Window NT to implement a FIFO page replacement policy yet get behavior similar to a LRU algorithm.

5. (6 points) For each of the following hardware changes, state what the effect would be on the internal and external fragmentations of the main memory:

   a) Increasing the virtual memory page size in a pure paging scheme.

   b) Converting from a pure segmentation segment to a pure paging scheme.

6. (12 points) For each of the following claims, argue if the claim is true or false. Be sure to include your justification.
   a) A CPU scheduler using lottery scheduling is well suited for a real-time system.

   b) Using lock ranks eliminates deadlocks involving locks.

   c) Given an ideal CPU scheduler (i.e. one that could predict the future, etc.) a system would not need locks.

7. (4 points) Explain how a larger page size can result in more “false sharing” in a Distribute Shared memory (DSM) system.