Homework Assignment #2 for

EE392m - Control Engineering in Industry, Spring 2005

1. PID for sideways heat transfer

A model for the sideways heat transfer was described in Lecture 2 (Slides 23 and 24) the step response data for the model were dealt with in Assignment 1, Problem 4. An IIR model of the impulse response is computed as described in Lecture 2, Slide 24 by sampling the continuous-time pulse response data at 1 sec interval. This model corresponds to the following sampled-time transfer function

```
      1.797e-009 z^4 + 0.00017 z^3 + 0.003674 z^2 + 0.006498 z + 0.001904
      ------------------------------------------------------------------
              z^5 - 2.338 z^4 + 1.97 z^3 - 0.7206 z^2 + 0.1008 z
```

Design a continuous-time controller for the system that will ensure the heat flux settling to a setpoint in about 20 s with minimal overshoot. Consider a digital (sampled time) implementation of the designed PID controller. Use discrete time simulation with the above described model to validate the design and demonstrate the performance. Produce plots of closed-loop responses of the output to the setpoint change (compare these to open loop step response plots), step response for the control input to the setpoint change in the closed loop, and step response to an input disturbance.

(a) Design a P controller by approximating the plant response by an integrator.
(b) Design a PI controller by adding an I loop to the P controller to remove the steady state error. Provide an initial estimate of the I gain from the cascaded design.
(c) Design a PID controller by adding a D term to your PI design and re-tuning. Evaluate the differentiating filter performance by applying it to the PI step response. What are the optimal PID gains? How much faster is the closed loop response to the setpoint compared to the open loop response? Explain how the closed-loop disturbance rejection compares to the open loop – illustrate by frequency response analysis (Bode plot).

Hint

Using Matlab functions `tf`, `step`, and `feedback` might save you some time

2. Disk drive

Consider the disk head control problem described in Matlab Control Systems Toolbox demo diskdemo.m.
In last few releases of Matlab, this demo can be accessed by typing `demo` at the Matlab prompt and then navigating to Toolboxes→Control Systems→Case Studies→Digital Servo Control of a Hard-Disk Drive.
Go through the demo to familiarize yourself with the problem statement and the solution proposed in the demo.
The assignment is to design a PID controller for this problem. The PID design can ignore most of the reasoning in the demo except the most pertinent specifications as described below.

To relieve you from the need to hack the demo, the problem relevant code from the demo and the baseline controller designed in the demo are given in the files `diskPID.m, diskdemo.mat` posted at the course website. After running the script `diskPID.m,` the following useful data is left in the workspace

```
%   Ts  - sampling time
%   Gd  - nominal sampled-time model
%   Gr  - rigid-body model (no flex modes)
%   Gdm - array of 16 perturbed models for Monte Carlo analysis
%   notchd - notch filter to filter out the flexible resonance
%   C2  - 4-th order controller designed in the demo
%       - use C2 as a baseline to compare with your design
```

To improve performance, the PID controller should work with the filtered plant output. Use the sampled-time notch filter `notchd` designed in the demo and connect it in series with the plant `Gd` to provide the filtered plant output for the control. To demonstrate the robustness of designed PID controller, use an array `Gdm` of the perturbed models for Monte Carlo analysis of the step disturbance rejection. Follow the Monte Carlo robustness analysis logic of the demo and apply it to your PID controller.

(a) Design a discrete time PID controller (using the notch filter `notchd`) that provides at least the same performance as the 'good' 4th-order controller C2 designed in the demo. The performance should be determined as the disturbance rejection step response both for the nominal plant and the 16 Monte Carlo perturbations of the nominal plant. What are the PID gains of the designed controller? Show the simulation results. If your PID design is right, the obtained performance should be better than for C2.
(b) Briefly describe the approach you took to find the PID gains and the reason for using this approach.

Hint
There are many 'right' approaches, lecture notes describe several (trial and error, cascaded loop design, optimization), use any one of them. The two important things are (i) performance – optimize it (ii) your design effort – minimize it.

3. PLL loop controller design
(This is a bonus problem providing points beyond the 100%)
Consider the PLL loop phase signal model (Lecture 4, Slides 10--11)

$$\dot{\theta} = d - K_o u$$
$$e = K_d \sin(\theta)$$

Assume that in this model $K_o = 1; K_d = 1$. The loop (and its low-pass filters) is desiged to work with a carrier signal around 2Mhz. The PLL phase should converge in about 100μs leaving enough room for the low-pass filtering effects to be left outside of the closed-loop bandwidth.

(a) Design a PI controller (loop filter) for the PLL to satisfy the above specification for the linearized model and provide a transient with no oscillations. What are the feedback gains of the controller?
(b) Produce simulation results for PLL phase transient with the designed controller (a) when the carrier frequency experiences sudden 60Khz step change. Simulate and compare the transients for the linearized and nonlinear models.

Hint
You can use Matlab `ode45` function for the nonlinear simulation